256Mb HyperRAM 3.0 x16 pSRAM

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1. FEATURES

- Interface: HyperBus-Extend-IO (HyperRAM 3.0)
- Power supply: 1.7V~2.0V
- Maximum clock rate: 250MHz
- Double-Data Rate (DDR) Up to 1000 MB/s
- Clock:
  - Single ended clock (CK)
  - Differential clock (CK/CK#)
- Chip Select (CS#)
- 16-bit data bus (DQ[15:0])
- Hardware reset (RESET#)
- Read-Write Data Strobe (RWDS[1:0])
  - Bidirectional Data Strobe / Mask
  - Output at the start of all transactions to indicate refresh latency
  - Output during read transactions as Read Data Strobe
  - Input during write transactions as Write Data Mask

Performance and Power

- Configurable output drive strength
- Power Saving Modes
  - Hybrid Sleep Mode
  - Deep Power Down
- Configurable Burst Characteristics
  - Linear burst
  - Wrapped burst lengths:
    - 16 (8 clocks)
    - 32 (16 clocks)
    - 64 (32 clocks)
    - 128 (64 clocks)
  - Hybrid burst - one wrapped burst followed by linear burst
- Array Refresh Modes
  - Full Array Refresh
  - Partial Array Refresh
- Operating temperature range:
  -40°C ≤ TCASE ≤ 85°C

2. ORDER INFORMATION

Part Number	VCC/VCCQ	I/O Width	Interface	Others
W958D6NWSX5I	1.8V	16	HyperBus-Extend-IO (HyperRAM 3.0)	WLCSP 30 ball, 200MHz, -40°C~85°C
W958D6NWSX4I	1.8V	16	HyperBus-Extend-IO (HyperRAM 3.0)	WLCSP 30 ball, 250MHz, -40°C~85°C

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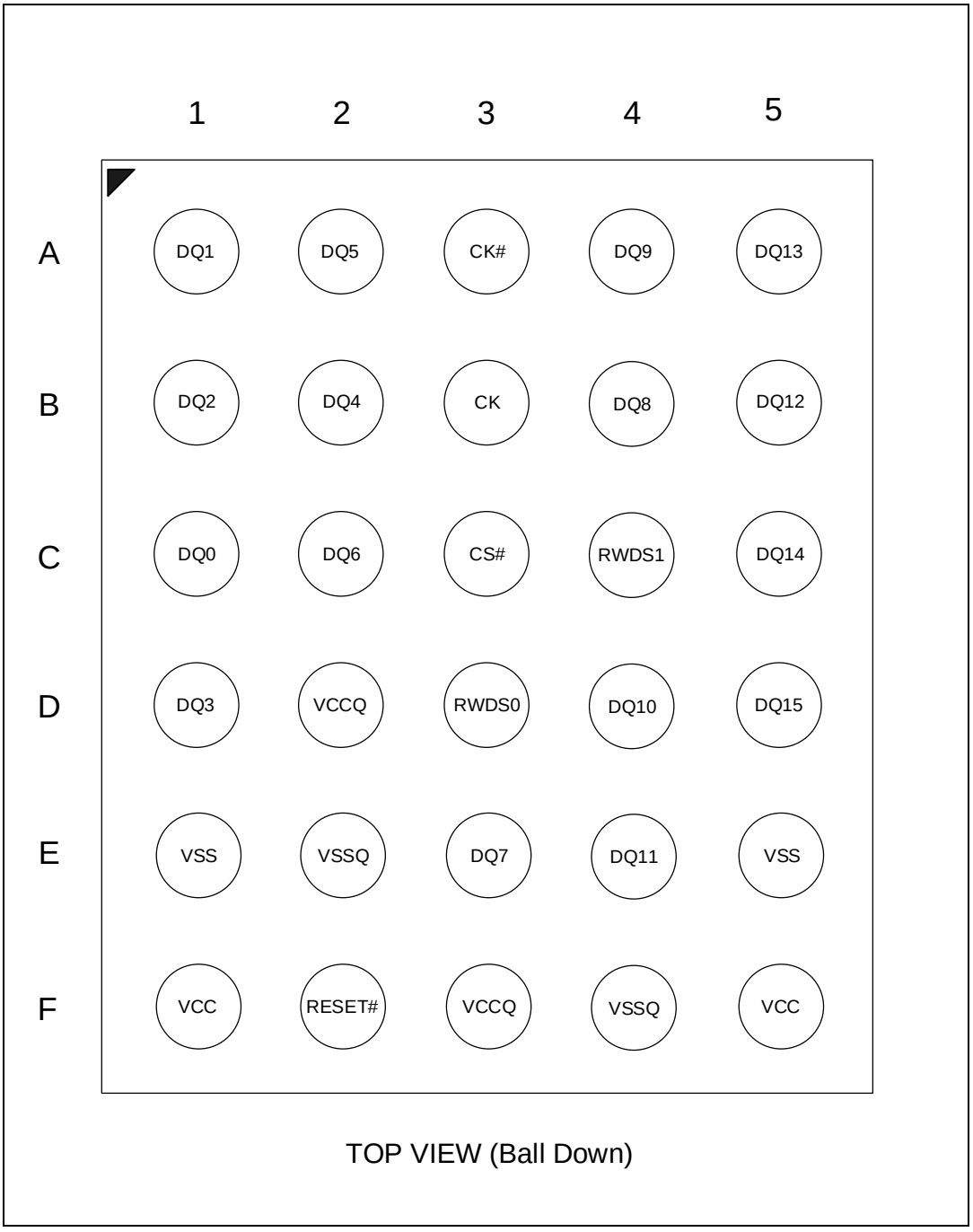
3. BALL ASSIGNMENT



WLCSP 30 Balls, Top View

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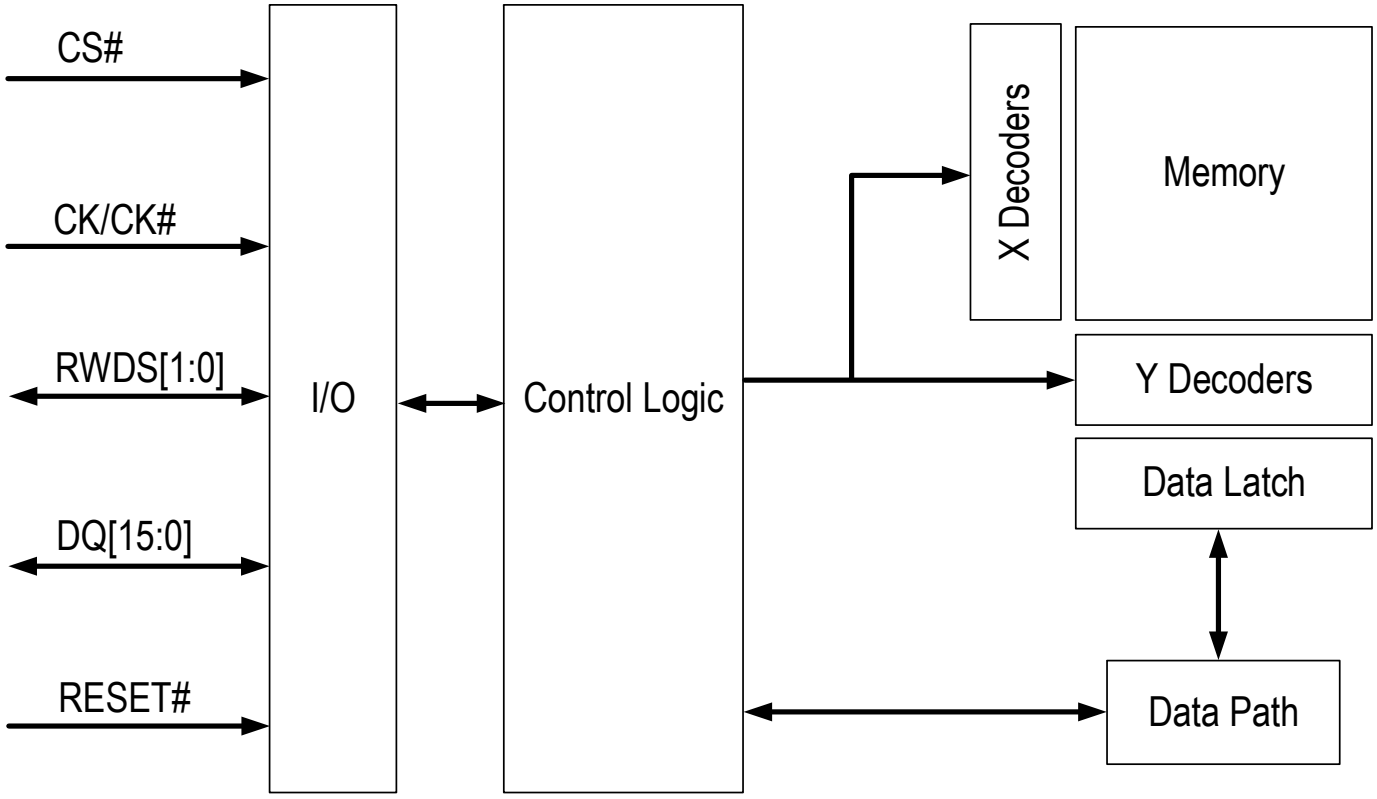
4. BALL DESCRIPTIONS

Signal Name	Type	Description
CS#	Input	**Chip Select:** Bus transactions are initiated with a High to Low transition. Bus transactions are terminated with a Low to High transition. The master device has a separate CS# for each slave.
CK, CK#	Input	**Differential Clock:** Command, address, and data information is output with respect to the crossing of the CK and CK# signals. **Single Ended Clock:** CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
DQ[15:0]	Input / Output	**Data Input / Output:** DQ[7:0] for Command, Address, and Data information are transferred on these signals during Read and Write transactions. DQ[15:8] for Data information are transferred on these signals during Read and Write transactions. Host has to drive DQ[15:8] all to “H” or “L” during the CA period. Floating is not allowed.
RWDS[1:0]	Input / Output	**Read Write Data Strobe:** During the Command/Address portion of all bus transactions RWDS is a slave output and indicates whether additional initial latency is required. Slave output during read data transfer, data is edge aligned with RWDS. Slave input during data transfer in write transactions to function as a data mask. RWDS[0] individually corresponds to the data on DQ[7:0] RWDS[1] individually corresponds to the data on DQ[15:8] RWDS High indicates additional latency, Low indicates no additional latency.
RESET#	Input, Internal Pull-up	**Hardware Reset:** When Low the slave device will self-initialize and return to the Standby state. RWDS[1:0] and DQ[15:0] are placed into the High-Z state when RESET# is Low. The slave RESET# input includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the High state.
V_{CC}	Power Supply	**V_{CC} Power Supply:** For supplying input buffer of CK/CK#, CS#, RESET#, DQ[15:0] and RWDS[1:0] internal circuitry and memory array.
V_{CCQ}	Power Supply	**V_{CCQ} Power Supply:** For supplying output buffer of DQ[15:0] and RWDS[1:0].
V_{SS}	Power Supply	**V_{SS} Ground:** Ground of V_{CC}.
V_{SSQ}	Power Supply	**V_{SSQ} Ground:** Ground of V_{CCQ}.

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

6.1 General Description

HyperRAM is a pSRAM device with HyperBus or HyperBus-Extend-IO, both are low signal count, Double Data Rate (DDR) interfaces. The DDR protocol transfers two 8-bit or two 16-bit data per clock cycle on the DQ input/output pins. HyperBus consists 8-bit wide DQ signals, a 16-bit wide data can be transferred in one clock cycle and HyperBus-Extend-IO consists 16-bit wide DQ signals, a 32-bit wide data can be transferred in one clock cycle. All inputs and outputs are LV-CMOS compatible. Each HyperRAM devices may have different features depends on its device names. For example, HyperRAM 3.0. The HyperRAM 3.0 device is one of HyperRAM devices with low signal count including 16 DQ pins, Double Data Rate (DDR) HyperBus-Extend-IO interface, that achieves much higher speed read and write throughput.

6.2 HyperBus-Extend-IO

The DDR protocol transfers two 16-bit data per clock cycle on the DQ input/output signals. A read or write transaction on HyperBus-Extend-IO consists of a series of 32-bit wide, one clock cycle data transfers at the internal array with two corresponding 16-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible. Command, address, and data information is transferred over the sixteen HyperBus-Extend-IO DQ[15:0] signals. The clock (CK#, CK) is used for information capture by a HyperBus-Extend-IO slave device when receiving command, address, or data on the DQ signals. Command or Address values are center aligned with clock transitions.

Every transaction begins with the assertion of CS# and Command-Address (CA) signals, followed by the start of clock transitions to transfer six CA bytes, followed by initial access latency and either read or write data transfers, until CS# is de-asserted.

Read and write transactions require two clock cycles to define the target row address and burst type, then an initial access latency of t_{ACC}. During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time (t_{RFH}) is added to the initial latency; by driving the RWDS signal to the High state. During the CA period the third clock cycle will specify the target data(32-bits) address within the target row. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequenced. When configured in linear burst mode, the device will automatically fetch the next sequential row from the memory array to support a continuous linear burst. Simultaneously accessing the next row in the array while the read or write data transfer is in progress, allows for a linear sequential burst operation.

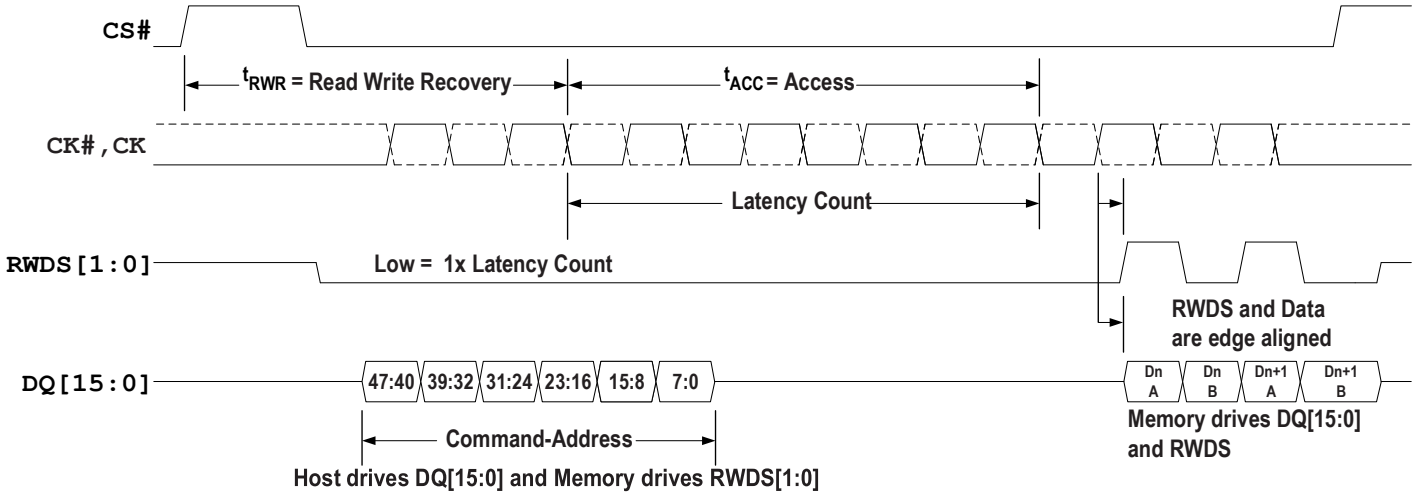


Figure 1 - Read Transaction, Single Initial Latency Count

Note: DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

The Read/Write Data Strobe (RWDS[1:0]) are bidirectional signals that indicates:

- When data will start to transfer from a HyperRAM device to the master device in read transactions (initial read latency)
- When data is being transferred from a HyperRAM device to the master device during read transactions (as a source synchronous read data strobe)
- When data may start to transfer from the master device to a HyperRAM device in write transactions (initial write latency)
- Data masking during write data transfers

During the CA transfer portion of a read or write transaction, RWDS[1:0] acts as an output from a HyperRAM device to indicate whether additional initial access latency is needed in the transaction.
During read data transfers, RWDS[1:0] are read data strobe with data values edge aligned with the transitions of RWDS[1:0].

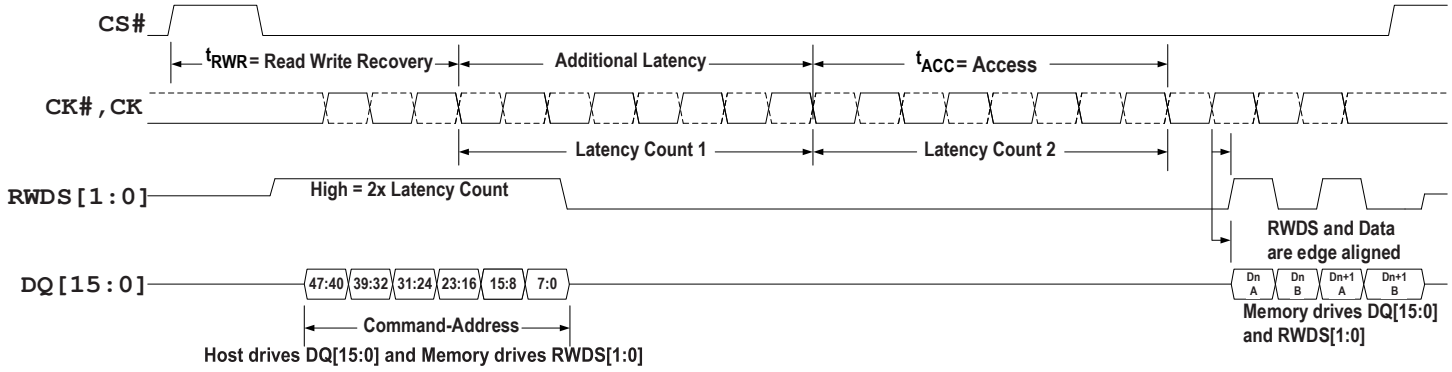


Figure 2 - Read Transaction, Additional Latency Count

During write data transfers, RWDS indicates whether each data transfer is masked with RWDS High (invalid and prevented from changing the data location in a memory) or not masked with RWDS Low (valid and written to a memory). Data masking may be used by the host to byte align write data within a memory or to enable merging of multiple non-word aligned writes in a single burst write. During write transactions, data is center aligned with clock transitions.

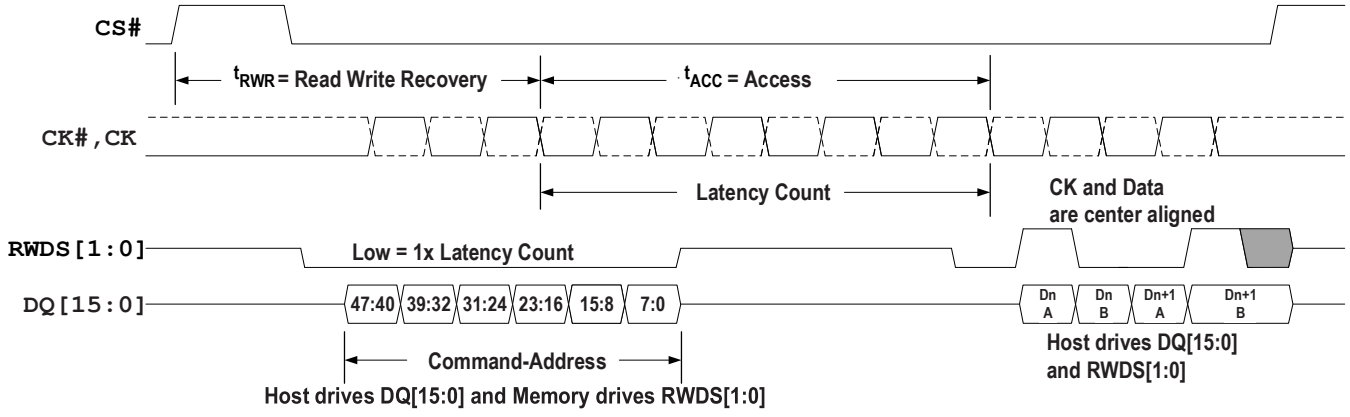


Figure3 - Write Transaction, Single Initial Latency Count

Note: The last write data can be masked or not masked.

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Read and write transactions are burst oriented, transferring the next sequential 32-bits during each clock cycle. Each individual read or write transaction can use either a wrapped or linear burst sequence.

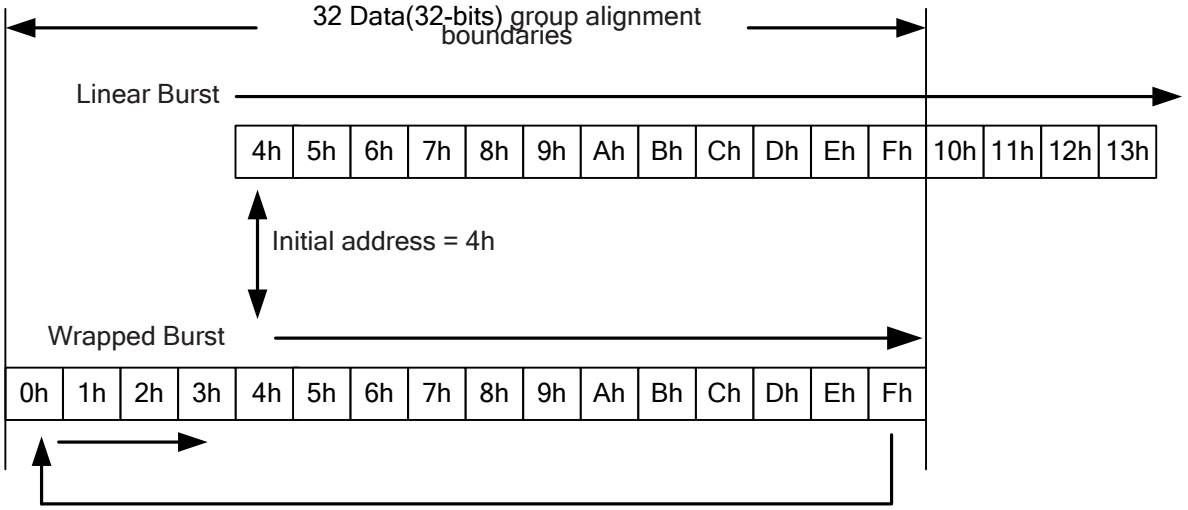

Figure 4 - Linear Versus Wrapped Burst Sequence

During wrapped transactions, accesses start at a selected location and continue to the end of a configured 32-bits group aligned boundary, then wrap to the beginning location in the group, then continue back to the starting location. Wrapped bursts are generally used for critical 32-bits first cache line fill read transactions. During linear transactions, accesses start at a selected location and continue in a sequential manner until the transaction is terminated when CS# returns High. Linear transactions are generally used for large contiguous data transfers such as graphic images. Since each transaction command selects the type of burst sequence for that transaction, wrapped and linear bursts transactions can be dynamically intermixed as needed.

7. HyperBus-Extend-IO TRANSACTION DETAILS

7.1 Command/Address Bit Assignments

All HyperBus-Extend-IO transactions can be classified as either read or write. A bus transaction is started with CS# going Low with clock in idle state (CK=Low and CK#=High). The first three clock cycles transfer three words of Command/Address (CA0, CA1, CA2) information to define the transaction characteristics. The Command/Address words are presented with DDR timing, using the first six clock edges. The following characteristics are defined by the Command/Address information:

- Read or Write transaction
- Address Space: memory array space or register space
  – Register space is used to access Device Identification (ID) registers and Configuration Registers (CR) that identify the device characteristics and determine the slave specific behavior of read and write transfers on the HyperBus-Extend-IO.
- Whether a transaction will use a linear or wrapped burst sequence
- The target row (and half-page) address (upper order address)
- The target column (word within half-page) address (lower order address)

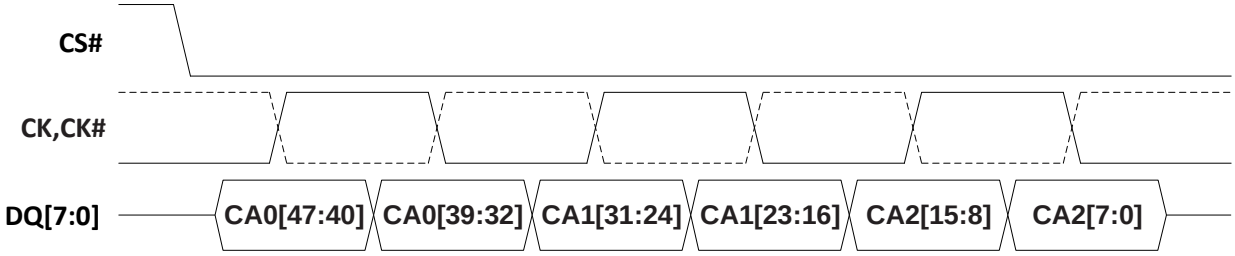

Figure 5 - Command-Address (CA) Sequence

Notes:

1. Figure shows the initial three clock cycles of all transactions on the HyperBus-Extend-IO.
2. CK# of differential clock is shown as dashed line waveform.
3. CA information is “center aligned” with the clock during both Read and Write transactions.
4. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.
5. In command/Address phase, DQ[15:8] input will be not used for command/Address decoding, however, the controller has to drive DQ[15:8] to “H” or “L”.

Table 1 - CA Bit Assignment to DQ Signals

Signal	CA0[47:40]	CA0[39:32]	CA1[31:24]	CA1[23:16]	CA2[15:8]	CA2[7:0]
DQ[7]	CA[47]	CA[39]	CA[31]	CA[23]	CA[15]	CA[7]
DQ[6]	CA[46]	CA[38]	CA[30]	CA[22]	CA[14]	CA[6]
DQ[5]	CA[45]	CA[37]	CA[29]	CA[21]	CA[13]	CA[5]
DQ[4]	CA[44]	CA[36]	CA[28]	CA[20]	CA[12]	CA[4]
DQ[3]	CA[43]	CA[35]	CA[27]	CA[19]	CA[11]	CA[3]
DQ[2]	CA[42]	CA[34]	CA[26]	CA[18]	CA[10]	CA[2]
DQ[1]	CA[41]	CA[33]	CA[25]	CA[17]	CA[9]	CA[1]
DQ[0]	CA[40]	CA[32]	CA[24]	CA[16]	CA[8]	CA[0]

Table 2 - Command/Address Bit Assignments

CA Bit#	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W#=1 indicates a Read transaction R/W#=0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS=0 indicates memory space AS=1 indicates the register space The register space is used to access device ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type=0 indicates wrapped burst Burst Type=1 indicates linear burst
44-16	Row & Upper Column Address	Row & Upper Column component of the target address: System data address bits A31-A3 Any upper Row address bits not used by a particular device density should be set to 0 by the host controller master interface. The size of Rows and therefore the address bit boundary between Row and Column address is slave device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are don't care in current HyperBus devices but should be set to 0 by the host controller master interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System data address bits A2-A0 selecting the starting data(32-bits) within a half-page.

Notes:

1. The Column address selects the burst transaction starting data location within a Row. The Column address is split into an upper and lower portion. The upper portion selects an 8 data(32-bits) Half-page and the lower portion selects the 32-bits within a Half-page where a read or write transaction burst starts.
2. The initial read access time starts when the Row and Upper Column (Half-page) address bits are captured by a slave interface. Continuous linear read burst is enabled by memory devices internally interleaving access to 8 data(32-bits) half-pages.

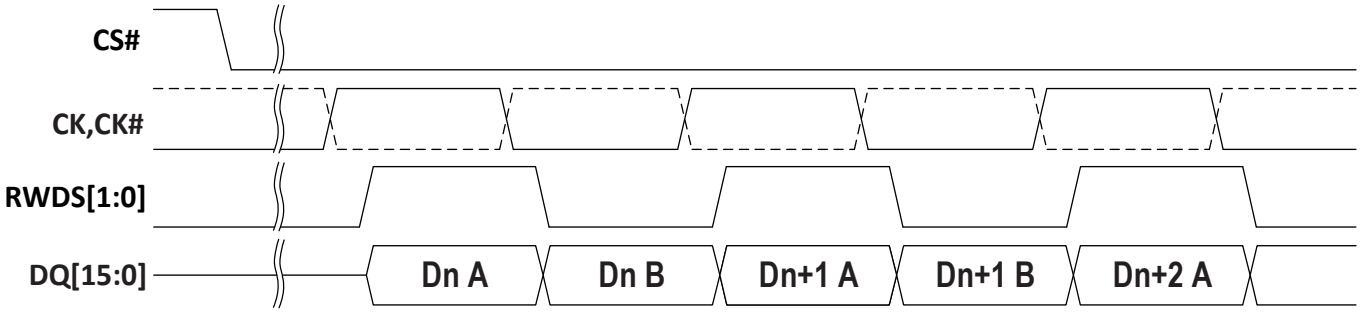

Figure 6 - Data Placement during a Read Transaction

Notes:

1. Figure shows a portion of a Read transaction on the HyperBus-Extend-IO. CK# of differential clock is shown as dashed line waveform.
2. Data is “edge aligned” with the RWDS serving as a read data strobe during read transactions.
3. Data is always transferred in full 32-bits increments (32-bits granularity transfers).
4. The address increments in each clock cycle. Dn A(16-bits) is between RWDS rising and falling edges and is followed by Dn B(16-bits) between RWDS falling and rising edges, of each 32-bit data.
5. Each 16-bits data always in high to low order with bit 15 on DQ15 and bit 0 on DQ0.

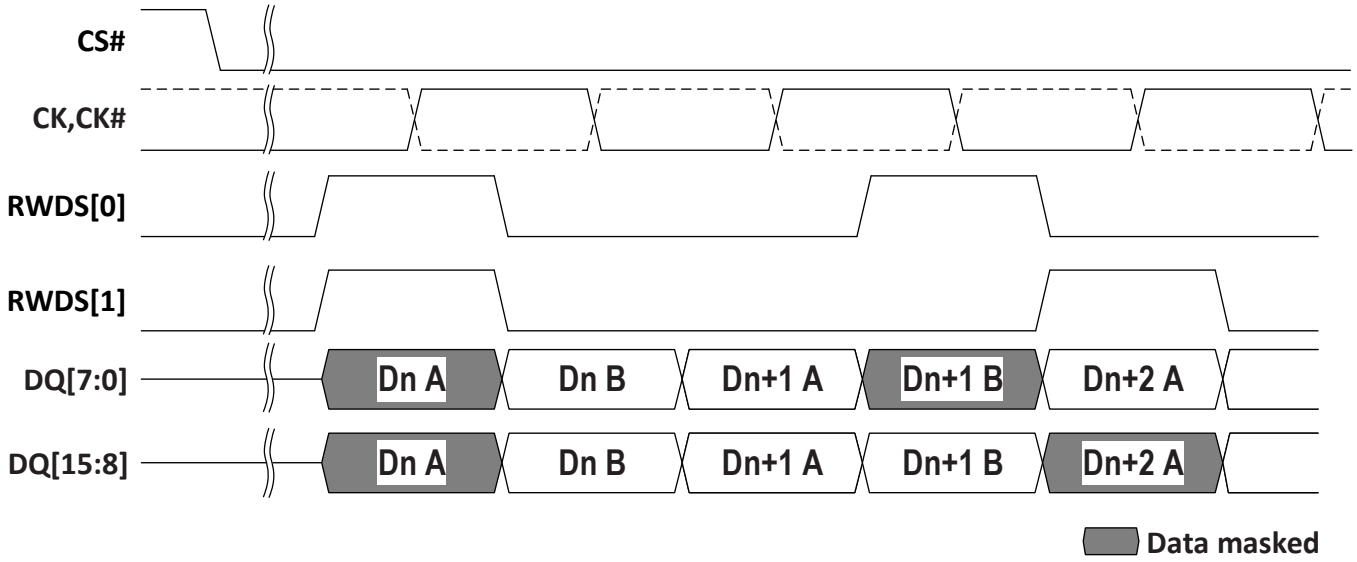

Figure 7 - Data Placement during a Write Transaction

Notes:

1. Figure shows a portion of a Write transaction on the HyperBus-Extend-IO.
2. Data is “center aligned” with the clock during a Write transaction.
3. RWDS[1:0] functions as a data mask during write data transfers with initial latency.
   RWDS[0] as a input data mask for the data on DQ0-7.
   RWDS[1] as a input data mask for the data on DQ8-15.

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7.2 Read Transactions

The HyperBus-Extend-IO master begins a transaction by driving CS# Low while clock is idle. The clock then begins toggling while CA words are transferred.

In CA0, CA[47] = 1 indicates that a Read transaction is to be performed. CA[46] = 0 indicates the memory space is being read or CA[46] = 1 indicates the register space is being read. CA[45] indicates the burst type (wrapped or linear). Read transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA[15:0]) identifies the target Word address within the chosen row.

The HyperBus-Extend-IO master then continues clocking for a number of cycles defined by the latency count setting in Configuration Register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed the memory starts to simultaneously transition the Read-Write Data Strobe (RWDS) and output the target data.

New data is output edge aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is Low. However, the HyperRAM device may stop RWDS transitions with RWDS Low, between the deliveries of words, in order to insert latency between words when crossing memory array boundaries.

Wrapped bursts will continue to wrap within the burst length and linear burst will output data in a sequential manner across row boundaries. When a linear burst read reaches the last address in the array, continuing the burst beyond the last address will provide data from the beginning of the address range. Read transfers can be ended at any time by bringing CS# High when the clock is idle.

The clock is not required to be free-running. The clock may remain idle while CS# is High.

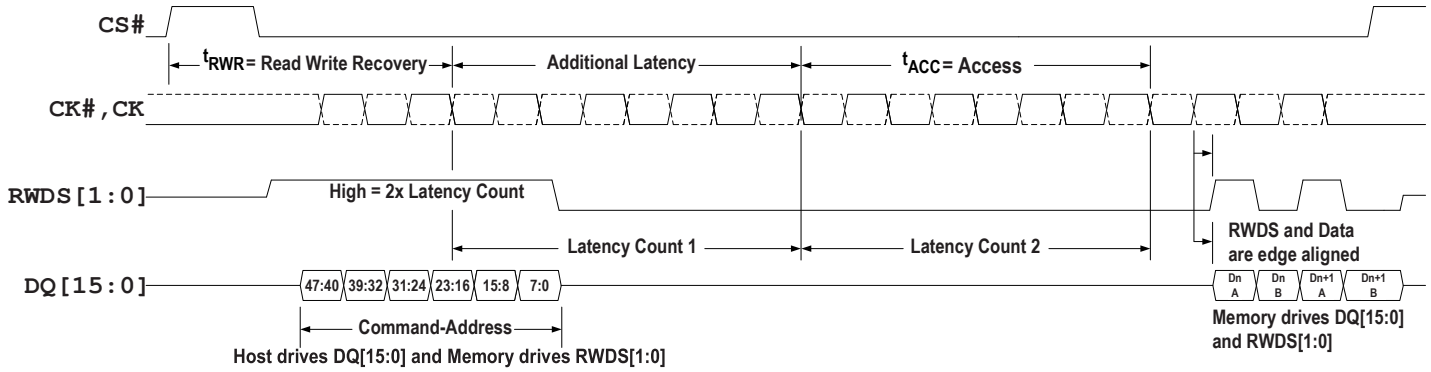

Figure 8 - Read Transaction with Additional Initial Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low and CK#=High.
2. CS# must return High before a new transaction is initiated.
3. CK# is the complement of the CK signal.CK# of a differential clock is shown as a dashed line waveform.
4. Read access array starts once CA[23:16] is captured.
5. The read latency is defined by the initial latency value in a configuration register.
6. In this read transaction example the initial latency count was set to four clocks.
7. In this read transaction RWDS High indication during CA delays output of target data by an additional four clocks.
8. The memory device drives RWDS during read transactions.
9. For register read, the output data Dn A[7:0] is RG[15:8], Dn B[7:0] is RG[7:0], Dn+1 A[7:0] is RG[15:8], Dn+1 B[7:0] is RG[7:0].
10. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to “H” or “L”.

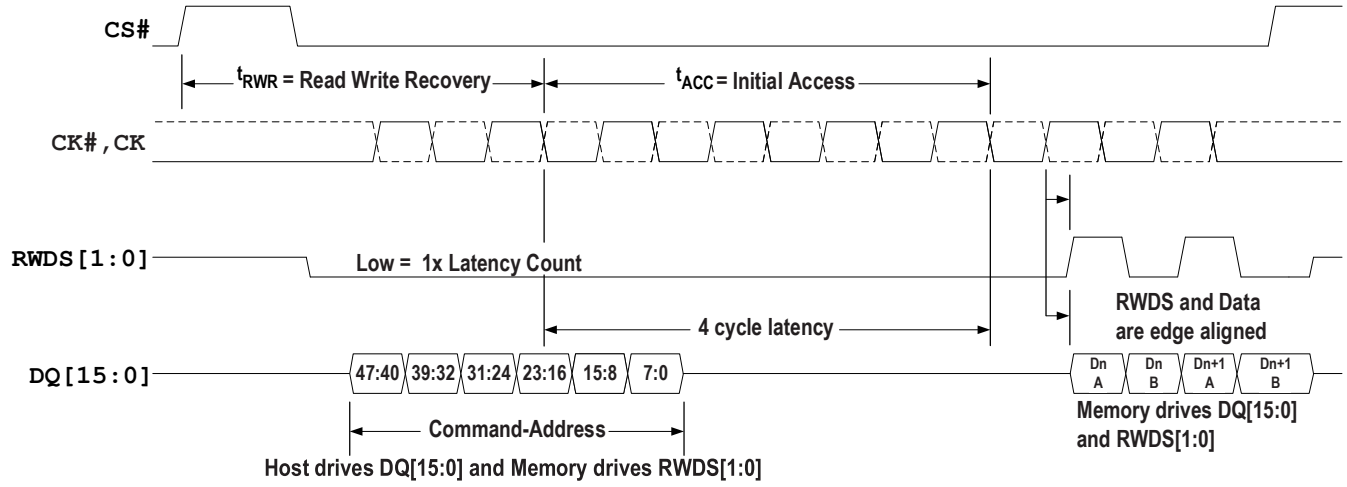

Figure 9 - Read Transaction without Additional Initial Latency

Notes:

1. RWDS is Low during the CA cycles. In this Read Transaction there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.
2. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to “H” or “L”.

7.3 Write Transactions (Memory Array Write)

The HyperBus-Extend-IO master begins a transaction by driving CS# Low while clock is idle. Then the clock begins toggling while CA words are transferred.

In CA0, CA[47] = 0 indicates that a Write transaction is to be performed. CA[46] = 0 indicates the memory space is being written. CA[45] indicates the burst type (wrapped or linear). Write transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA[15:0]) identifies the target word address within the chosen row.

The HyperBus-Extend-IO master then continues clocking for a number of cycles defined by the latency count setting in configuration register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted.

Once these latency clocks have been completed the HyperBus-Extend-IO master starts to output the target data. Write data is center aligned with the clock edges. The first 16-bits data is captured by the memory on the rising edge of CK and the second 16-bits data is captured on the falling edge of CK.

During the CA clock cycles, RWDS is driven by the memory.

During the write data transfers, RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is High the data will be masked and the array will not be altered. When data is being written and RWDS is Low the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the HyperRAM device is able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Data will continue to be transferred as long as the HyperBus-Extend-IO master continues to transition the clock while CS# is Low. Legacy format wrapped bursts will continue to wrap within the burst length. Hybrid wrap will wrap once then switch to linear burst starting at the next wrap boundary. Linear burst accepts data in a sequential manner across page boundaries. Write transfers can be ended at any time by bringing CS# High when the clock is idle.

When a linear burst write reaches the last address in the memory array space, continuing the burst will write to the beginning of the address range.

The clock is not required to be free-running. The clock may remain idle while CS# is High.

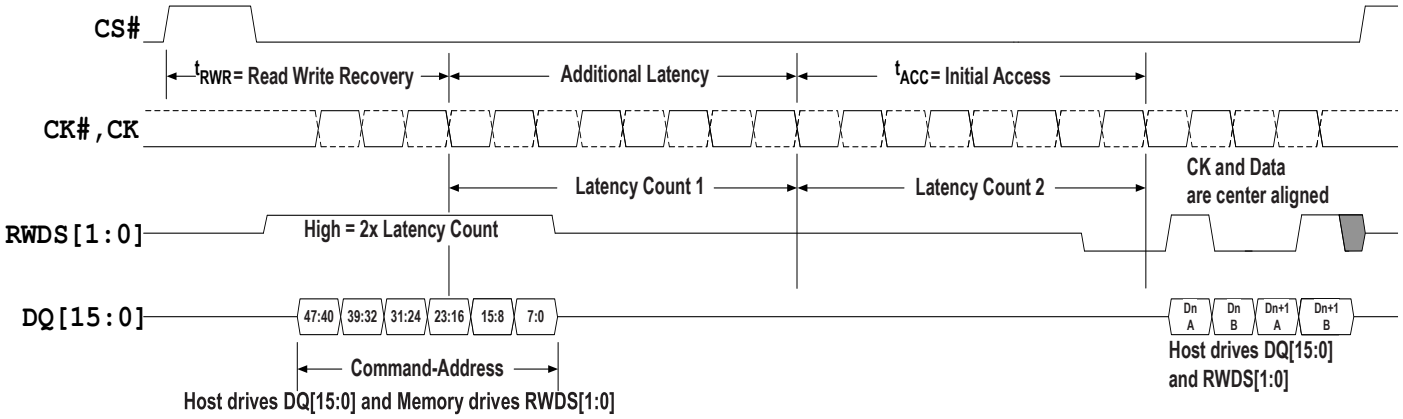

Figure 10 - Write Transaction with Additional Initial Latency

Notes:

1. Transactions must be initiated with CK=Low and CK#=High.
2. CS# must return High before a new transaction is initiated.
3. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
4. In this example, RWDS indicates that additional initial latency cycles are required.
5. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus-Extend-IO master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
6. During data transfer, RWDS is driven by the host to indicate which data should be either masked or loaded into the array.
7. The figure shows RWDS masking Dn A and Dn+1 B to perform an unaligned data write to Dn B and Dn+1 A.
8. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

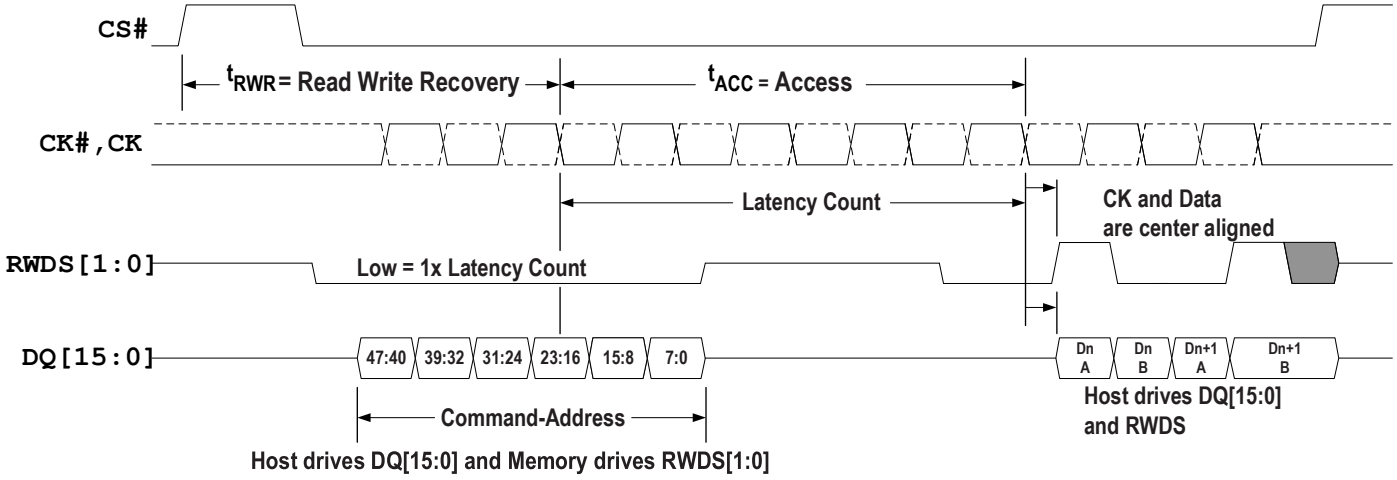

Figure 11 - Write Transaction without Additional Initial Latency

Notes:

1. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
2. In this example, RWDS indicates that there is no additional latency required.
3. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus-Extend-IO master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
4. During data transfer, RWDS is driven by the host to indicate which data should be either masked or loaded into the array.
5. The figure shows RWDS masking Dn A and Dn+1 B to perform an unaligned data write to Dn B and Dn+1 A.
6. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

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7.4 Write Transactions without Initial Latency (Register Write)

A Write transaction starts with the first three clock cycles providing the Command/Address information indicating the transaction characteristics. CA0 may indicate that a Write transaction is to be performed and also indicates the address space and burst type (wrapped or linear).

Writes without initial latency are used for register space writes. HyperRAM device write transactions with zero latency mean that the CA cycles are followed by write data transfers. Writes with zero initial latency, do not have a turnaround period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the HyperRAM device has received the first byte of CA i.e. before the HyperRAM device knows whether the transaction is a read or write to register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the CA period in this case, the HyperRAM device may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All write data are written.

The first 16-bits data is presented on the rising edge of CK and the second 16-bits data is presented on the falling edge of CK. Write data is center aligned with the clock inputs. Write transfers can be ended at any time by bringing CS# High when clock is idle. The clock is not required to be free-running.

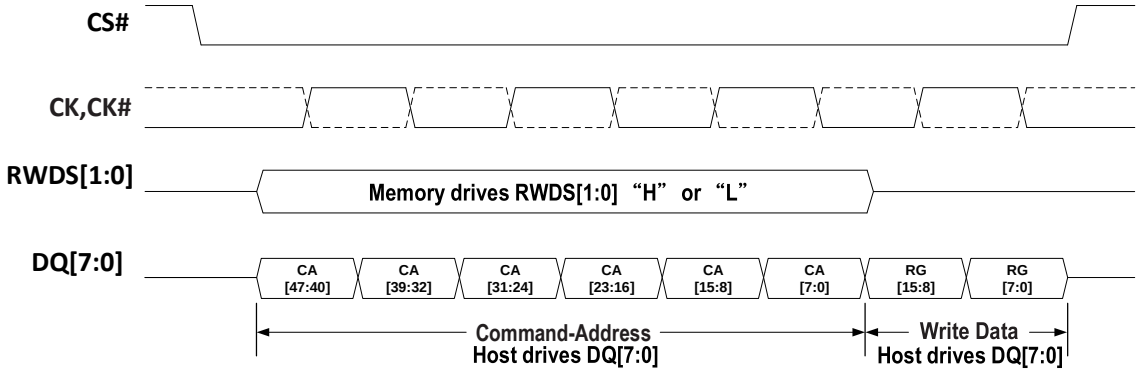

Figure 12 - Write Operation without Initial Latency (Register Write)

Notes:

1. RWDS not driven by the master during write data transfers with zero initial latency. Full data are always written in this case. RWDS may be driven Low or left High-Z by the slave during write data transfer.
2. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

8. MEMORY SPACE

8.1 HyperRAM Memory Space addressing

Table 3 - Memory Space Address Map (data based – 32-bits)

Unit Type	Count	System Word Address Bits	CA Bits	Notes
Rows within 256 Mb device	32768 (Rows)	A22~A8	35~21	
Row	1 (row)	A7~A3	20~16	256 (32-bits addresses) 1K bytes
Half-Page	8 (32 bits addresses)	A2~A0	2~0	8 (32-bits addresses) 32 bytes

Table 4 - Memory Space Address Map (data based – 32-bits)

		256Mb
Row Address	System Data Address Bits	A22~A8
	CA Bits	35~21
Column Address	System Data Address Bits	A7~A0
	CA Bits	20~16; 2~0
Half-Page (HP) Address	System Data Address Bits	A7~A3
	CA Bits	20~16
Word of HP Address	System Data Address Bits	A2~A0
	CA Bits	2~0

Notes:

1. Each row has 32 Half-pages. Each Half-page has 8 data(32-bits). Each column has 256 data(32-bits) (1K bytes).
2. Half-Page address is also named as upper column address. 32-bits of HP address is also named as lower column address.

8.2 Density and Row Boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register.

A 256Mbit HyperRAM device has 8 column address bits and 15 row address bits for a total of 23 address bits for 32-bits address = 2^{23} x 32 = 8M x 32 = 256Mbit. The 8 column address bits indicate that each row holds 2^{8} x 32 = 8192 bits. The row address bit count indicates there are 32768 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

9. REGISTER SPACE

9.1 HyperRAM Register Addressing

Table 5 - Register Space Address Map

Register	System Address	—	—	—	31~27	26~19	18~11	10~3	—	2~0
	CA Bits	47	46	45	44~40	39~32	31~24	23~16	15~8	7~0
Identification Register 0 (read only)		C0h or E0h				00h	00h	00h	00h	00h
Identification Register 1 (read only)		C0h or E0h				00h	00h	00h	00h	01h
Configuration Register 0 Read		C0h or E0h				00h	01h	00h	00h	00h
Configuration Register 0 Write		60h				00h	01h	00h	00h	00h
Configuration Register 1 Read		C0h or E0h				00h	01h	00h	00h	01h
Configuration Register 1 Write		60h				00h	01h	00h	00h	01h

Notes:

1. When CA[46] is 1 a read or write transaction accesses the Register Space.
2. CA[45] may be either 0 or 1 for either wrapped or linear read. CA[45] must be 1 as only linear single word register writes are supported.
3. The Burst type (wrapped/linear) definition is not supported in Register Reads. Hence C0h/E0h have the same effect.

9.2 Register Space Access

Register default values are loaded upon power-up or hardware reset. The registers can be altered at any time while the device is in the standby state.

Loading a register is accomplished with write transaction without initial latency using a single 16-bits word write transaction.

Each register is written with a separate single word write transaction. Register write transactions have zero latency, the single word of data immediately follows the CA. RWDS is not driven by the host during the write because RWDS is always driven by the memory during the CA cycles to indicate whether a memory array refresh is in progress. Because a register space write goes directly to a register, rather than the memory array, there is no initial write latency, related to an array refresh that may be in progress. In a register write, RWDS is also not used as a data mask because both bytes of a register are always written and never masked.

Reserved register fields must be written with their default value. Writing reserved fields with other than default values may produce undefined results.

Note: The host must not drive RWDS during a write to register space.

Note: The RWDS signal is driven by the memory during the CA period based on whether the memory array is being refreshed. This refresh indication does not affect the writing of register data.

Note: The RWDS signal returns to high impedance after the CA period. Register data is never masked. Both data bytes of the register data are loaded into the selected register.

Reading of a register is accomplished with read transaction with single or double initial latency using a single 16 bit read transaction. If more than one word is read, the same register value is repeated in each word read. The contents of the register is returned in the same manner as reading array data, with one or two latency counts, based on the state of RWDS during the CA period. The latency count is defined in the Configuration Register 0 Read Latency field (CR0[7:4]).

9.3 Device Identification Registers

There are two read only, non-volatile, word registers, that provide information on the device selected when CS# is low. The device information fields identify:

- Manufacture
- Type
- Density
  - – Row address bit count
  - – Column address bit count

Table 6 - ID Register 0 Bit Assignments

Bits	Function	Settings (Binary)
[15:14]	Reserved	00b - (default)
[13]	Reserved	0b - (default)
[12:8]	Row Address Bit Count	01110b - Fifteen Row address bits
[7:4]	Column Address Bit Count	0111b - Eight column address bits
[3:0]	Manufacturer	**0110b - Winbond** Others - Reserved

Table 7 - ID Register 1 Bit Assignments

Bits	Function	Settings (Binary)
[15:4]	Reserved	0000_0000_0000b (default)
[3:0]	Device Type	1001b - HyperRAM 3.0 Others - Reserved

9.4 Configuration Register 0

Configuration Register 0 (CR0) is used to define the power state and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, or 128 data(16-bits) aligned and length data group)
- Wrapped Burst Type
  - – Legacy wrapped burst (sequential access with wrap around within a selected length and aligned group)
  - – Hybrid burst (Legacy wrapped burst once then linear burst at start of the next sequential group)
- Initial Latency
- Variable Latency
  - – Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down Mode

Table 8 - Configuration Register 0 Bit Assignments

CR0 Bit	Function	Settings (Binary)
[15]	Deep Power Down Enable	1b - Normal operation (default) 0b - Writing 0 to CR0[15] causes the device to enter Deep Power Down (DPD) Note: 1: HyperRAM will automatically set the value of CR0[15] to “1” after exit DPD.
[14:12]	Drive Strength	000b - 34 ohms (default) 001b - 115 ohms 010b - 67 ohms 011b - 46 ohms 100b - 34 ohms 101b - 27 ohms 110b - 22 ohms 111b - 19 ohms
[11:8]	Reserved	1b - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.
[7:4]	Initial Latency	0000b - 5 Clock Latency @ 133MHz Max Frequency 0001b - 6 Clock Latency @ 166MHz Max Frequency 0010b - 7 Clock Latency @ 200MHz Max Frequency (default) 0010b - 7 Clock Latency @ 250MHz Max Frequency 0011b - Reserved 0100b - Reserved ... 1101b - Reserved 1110b - 3 Clock Latency @ 85MHz Max Frequency 1111b - 4 Clock Latency @ 104MHz Max Frequency
[3]	Fixed Latency Enable	0b - Variable Latency – 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1b - Fixed 2 times Initial Latency (default)
[2]	Hybrid Burst Enable	0b: Wrapped burst sequences to follow hybrid burst sequencing 1b: Wrapped burst sequences in legacy wrapped burst manner (default)
[1:0]	Burst Length	00b - 128 01b - 64 10b - 16 11b - 32 (default)

9.4.1 Wrapped Burst

A wrapped burst transaction accesses memory within a group of data(16-bits) aligned on a 16-bits boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 data(16-bits) alignment and length. During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured 16-bits group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical 16-bits first instruction or data cache line fill read accesses.

9.4.2 Hybrid Burst

The beginning of a hybrid burst will wrap within the target address wrapped burst group length before continuing to the next half-page of data beyond the end of the wrap group. Continued access is in linear burst order until the transfer is ended by returning CS# High. This hybrid of a wrapped burst followed by a linear burst starting at the beginning of the next burst group, allows multiple sequential address cache lines to be filled in a single access. The first cache line is filled starting at the critical 16-bits. Then the next sequential line in memory can be read in to the cache while the first line is being processed.

Table 9 - CR0[2] Control of Wrapped Burst Sequence

Bit	Default Value	Name
2	1	Hybrid Burst Enable CR0[2]= 0b: Wrapped burst sequences to follow hybrid burst sequencing CR0[2]= 1b: Wrapped burst sequences in legacy wrapped burst manner

Table 10 - Example Wrapped Burst Sequences (HyperRAM Addressing)

Burst Type	Wrap Boundary (16-bits)	Start Address (Hex)	Address Sequence (Hex) of Data(32-bits)
Hybrid 128	128 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02 (Wrap complete, now linear beyond the end of the initial 128 wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, (Wrap complete, now linear beyond the end of the initial 64 wrap group) 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, (Wrap complete, now linear beyond the end of the initial 64 wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, (Wrap complete, now linear beyond the end of the initial 16 wrap group) 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, (Wrap complete, now linear beyond the end of the initial 16 wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
Hybrid 32	32 Wrap once then Linear	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09 (Wrap complete, now linear beyond the end of the initial 32 wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
Wrap 64	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, ...
Wrap 64	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...
Wrap 16	16	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, ...
Wrap 16	16	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, ...
Wrap 32	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...
Linear	Linear Burst	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...

9.4.3 Initial Latency

Memory Space read and writes transactions or Register Space read transactions require some initial latency to open the row selected by the CA. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the HyperRAM clock input frequency and can vary from 3 to 7 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 7 clocks, allowing for operation up to a maximum frequency of 250MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a Memory Space read or write transaction or Register Space read transaction begins, the RWDS signals goes High during the CA to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register Space write transactions always have zero initial latency. RWDS may be High or Low during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

9.4.4 Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS High during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh, it simply provides a fixed (deterministic) initial latency for all of these transaction types. The fixed latency option may simplify the design of some HyperBus-Extend-IO memory controllers or ensure deterministic transaction performance. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven High only when additional latency for a refresh is required.

9.4.5 Drive Strength

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] and RWDS signal output impedance to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the mid-point of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage (1.8V) and 50°C. The impedance values may vary from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

9.4.6 Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming state called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within t_{DPDIN} time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# Low then High, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. All register content might lost in Deep Power Down State.

9.5 Configuration Register 1

Configuration Register 1 (CR1) is used to define the refresh array size, refresh rate and Hybrid Sleep for the HyperRAM device. Configurable characteristics include:

- Partial Array Refresh
- Hybrid Sleep State
- Refresh Rate

Table 11 - Configuration Register 1 Bit Assignments

CR1 Bit	Function	Settings (Binary)
[15-8]	Reserved	FFh - Reserved (default) Reserved for Future Use. When writing this register, these bits should keep FFh for future compatibility.
[7]	Reserved	1b - Reserved (default) When writing this register, this bit should keep 1b.
[6]	Master Clock Type	1b - Single Ended - CK (default) 0b - Differential - CK#, CK
[5]	Hybrid Sleep	1b - Writing 1 to CR1[5] causes the device to enter Hybrid Sleep (HS) State 0b - Normal operation (default)
[4:2]	Partial Array Refresh	000b - Full Array (default) 001b - Bottom 1/2 Array 010b - Bottom 1/4 Array 011b - Bottom 1/8 Array 100b - Reserved 101b - Top 1/2 Array 110b - Top 1/4 Array 111b - Top 1/8 Array
[1:0]*[1]	Distributed Refresh Interval	10b - Reserved 11b - Reserved 00b - Reserved 01b - 4µS (t_{CSM})

Note:
1. CR1[1:0] is read only.

9.5.1 Master Clock Type

Two clock types, namely single ended and differential, are supported by HyperRAM. CR1[6] selects which type to use.

9.5.2 Partial Array Refresh

The partial array refresh configuration restricts the refresh operation in HyperRAM device to a portion of the memory array specified by CR1[4:2]. This reduces the standby current. The default configuration refreshes the whole array.

9.5.3 Hybrid Sleep

When the HyperRAM device is not needed for system operation, it may be placed in Hybrid Sleep state if data in the device needs to be retained. Enter Hybrid Sleep state by writing 1 to CR1[5]. Bringing CS# Low will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost.

9.5.4 Distributed Refresh Interval

The HyperRAM device is built with volatile memory array which requires periodic refresh of all bits in the array. The refresh operation can be done by an internal self-refresh logic that will evenly refresh the memory array automatically.

The automatic refresh operation can only be done when the memory array is not being actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS high during the CA period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The evenly distributed refresh operations requires a maximum refresh interval between two adjacent refresh operations. The maximum distributed refresh interval will varies with temperature as shown in Table 12 - Distributed Refresh Interval per Temperature.

Table 12 - Distributed Refresh Interval per Temperature

Device Temperature (T_{CASE} °C)	Maximum Distributed Refresh Interval (µS)	CR1[1:0]
T_{CASE} < 85	4	01b

The distributed refresh operation requires that the host does not do burst transactions longer than the distributed refresh interval to prevent the memory from unable doing the distributed refreshes operation when it is needed.

This sets an upper limit on the length of read and write transactions so that the automatic distributed refresh operation can be done between transactions. This limit is called the CS# low maximum time (t_{CSM}) and the t_{CSM} will be equal to the maximum distributed refresh interval.

The host system is required to respect the t_{CSM} value by ending each transaction before violating t_{CSM}. This can be done by host memory controller logic splitting long transactions when reaching the t_{CSM} limit, or by host system hardware or software not performing a single read or write transaction that would be longer than t_{CSM}.

As noted in Table 12 of distributed refresh interval, the maximum refresh interval is longer at lower temperatures such that t_{CSM} could be increased to allow longer transactions. The host system can either use the CR1[1:0] value from the table for the maximum operating temperature or, may determine the current operating temperature from a temperature sensor in the system in order to set a longer distributed refresh interval.

10. INTERFACE STATES

10.1 IO condition of interface states

Below Interface States table describes the required value of each signal for each interface state.

Table 13 - Interface States

Interface State	Vcc / VccQ	CS#	CK, CK#	DQ15-DQ0	RWDS[1:0]	RESET#
Power-Off	< V_{LKO}	X	X	High-Z	High-Z	X
Power-On (Cold) Reset	≥ Vcc / VccQ min	X	X	High-Z	High-Z	X
Hardware (Warm) Reset	≥ Vcc / VccQ min	X	X	High-Z	High-Z	L
Interface Standby	≥ Vcc / VccQ min	H	X	High-Z	High-Z	H
CA	≥ Vcc / VccQ min	L	T	Master Output Valid	X	H
Read Initial Access Latency (data bus turn around period)	≥ Vcc / VccQ min	L	T	High-Z	L	H
Write Initial Access Latency (RWDS turn around period)	≥ Vcc / VccQ min	L	T	High-Z	High-Z	H
Read data transfer	≥ Vcc / VccQ min	L	T	Slave Output Valid	Slave Output Valid X or T	H
Write data transfer with Initial Latency	≥ Vcc / VccQ min	L	T	Master Output Valid	Master Output Valid X or T	H
Write data transfer without Initial Latency *1	≥ Vcc / VccQ min	L	T	Master Output Valid	Slave Output L or High-Z	H
Active Clock Stop	≥ Vcc / VccQ min	L	Idle	Master or Slave Output Valid or High-Z	X	H
Deep Power Down	≥ Vcc / VccQ min	H	X or T	High-Z	High-Z	H
Hybrid Sleep	≥ Vcc / VccQ min	H	X or T	High-Z	High-Z	H

Legend

L = V_{IL}

H = V_{IH}

X = either V_{IL}, V_{IH}, V_{OL} or V_{OH}

L/H = rising edge

H/L = falling edge

T = Toggling during information transfer

Idle = CK is Low and CK# is High.

Valid = all bus signals have stable L or H level

Note:

1. Writes without initial latency (with zero initial latency), do not have a turnaround period for RWDS[1:0]. The HyperRAM device will always drive RWDS[1:0] during the CA period to indicate whether extended latency is required. Since master write data immediately follows the CA period the HyperRAM device may continue to drive RWDS[1:0] Low or may take RWDS[1:0] to High-Z. The master must not drive RWDS[1:0] during Writes with zero latency. Writes with zero latency do not use RWDS[1:0] as a data mask function. All write data are written.

10.2 Power Conservation Modes

10.2.1 Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS#= High). The HyperRAM device will stay at interface standby state when CS# = High, CK, CK# = 0 or 1, and RESET# = High. When the HyperRAM device staying at interface standby state, it will not drive the DQs pin and RWDS pin and only monitor the status of CS# and RESET# input pins.

10.2.2 Active Clock Stop

The Active Clock Stop state reduces device interface energy consumption to the I_{CC6} level during the data transfer portion of a read or write operation. The device automatically enables this state when clock remains stable for t_{ACC} + 30 nS. While in Active Clock Stop state, read data is latched and always driven onto the data bus. Active Clock Stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be Low throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 nS. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The Active Clock Stop state must not be used in violation of the t_{CSM} limit. CS# must go High before t_{CSM} is violated. Note that it is recommended to stop the clock when it is in Low state.

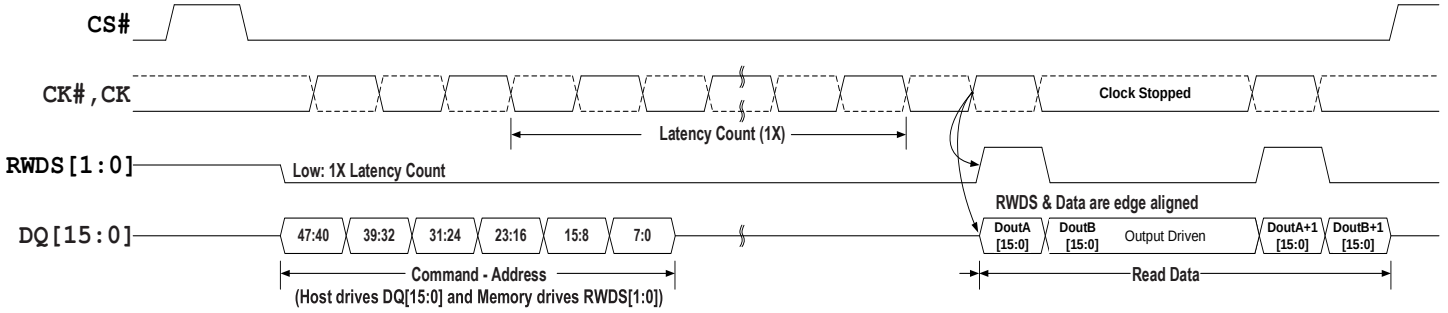

Figure 13 - Active Clock Stop during Read Transaction (DDR)

Note: DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

10.2.3 Hybrid Sleep

In the Hybrid Sleep (HS) state, the current consumption is reduced (I_{HS}). HS state is entered by writing a 1 to CR1[5]. The device reduces power within t_{HSIN} time. The data in Memory Space and Register Space is retained during HS state. Bringing CS# Low will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit HS state. Returning to Standby state requires t_{EXTHS} time. Following the exit from HS due to any of these events, the device is in the same state as entering HS.

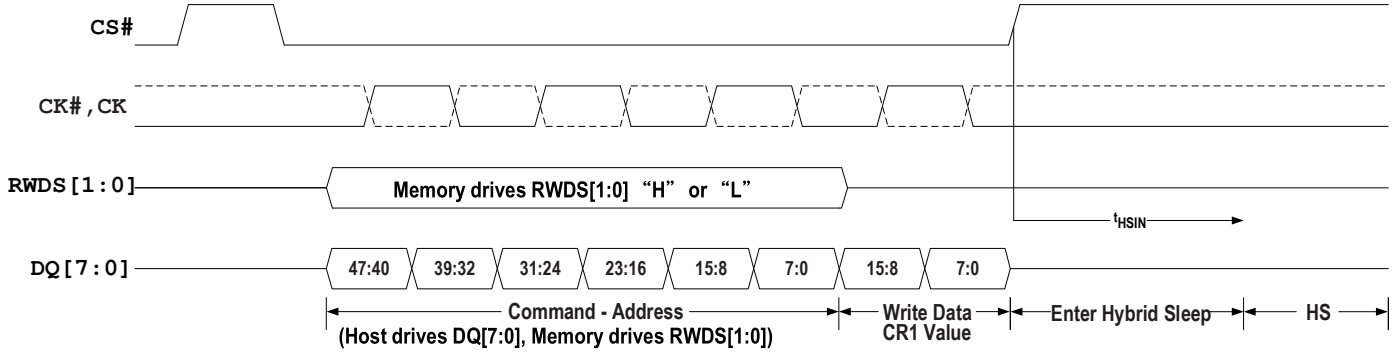

Figure 14 - Enter Hybrid Sleep Transaction

Note: DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

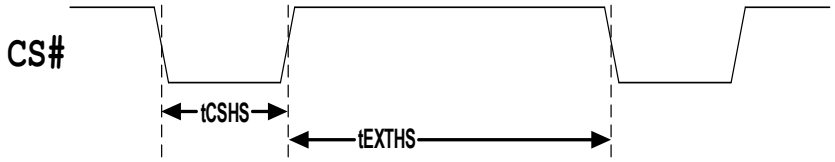

Figure 15 - Exit Hybrid Sleep Transaction

10.2.4 Deep Power Down

In the Deep Power down (DPD) state, current consumption is driven to the lowest possible level (I_{DPD}). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in Memory Space is lost, (becomes invalid without refresh) during DPD state. Driving CS# Low then High will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. Returning to Standby state requires t_{EXTDPD} time. Returning to Standby state following a POR requires t_{VCS} time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

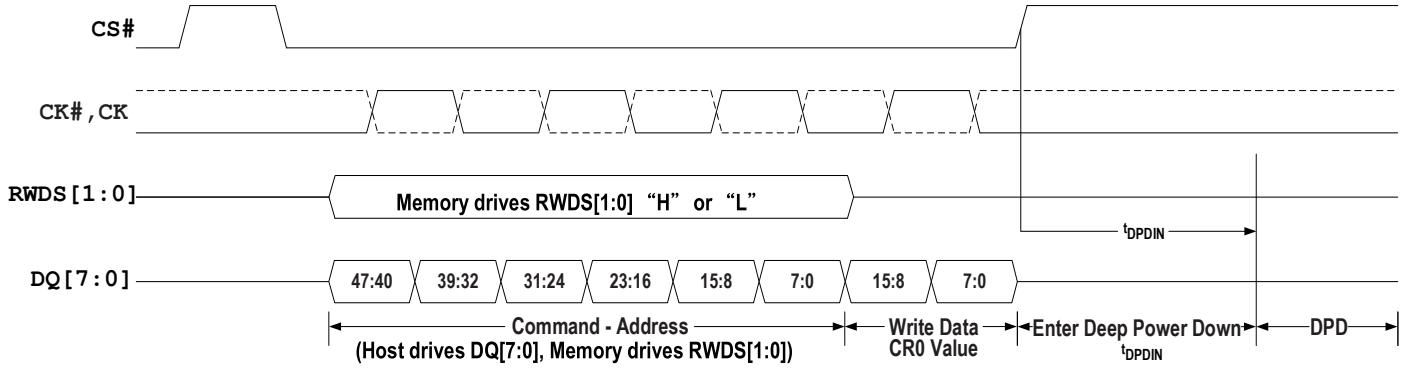

Figure 16 - Enter DPD Transaction

Note: DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

Figure 17 - Exit DPD Transaction

11. ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Voltage on V_{CC}, V_{CCQ} supply relative to V_{SS}	-0.5	V_{CC} +0.5	V	1
Voltage to any ball except V_{CC} relative to V_{SS}	-0.5	V_{CC} +0.5	V	1
Soldering temperature and time 10s (solder ball only)	+260		°C	1
Storage temperature (plastic)	-65	+150	°C	1
Output Short Circuit Current		100	mA	1, 2

Notes:

1. Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

11.2 Latch up Characteristics

Table 14 - Latch up Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	-1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SSQ} on all I/O connections	-1.0	V_{CCQ} + 1.0	V
V_{CCQ} Current	-100	+100	mA

Note:

1. Excludes power supplies V_{CC}/V_{CCQ}. Test conditions: V_{CC} = V_{CCQ}, one connection at a time tested, connections not being tested are at V_{SS}.

11.3 Operating Ranges

11.3.1 DC Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
V_{CC}, V_{CCQ}	Power Supply (typical 1.8V)		1.7	2.0	V
V_{IL}	Input Low Voltage		-0.15 x V_{CC}	0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	1.15 x V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA for DQ[15:0]	–	0.2	V
V_{OH}	Output High Voltage	I_{OH} = 100µA for DQ[15:0]	V_{CCQ} - 0.2	–	V

Note:

1. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the V_{CC}, V_{CCQ} operation condition out of range mentioned in above table.

11.3.2 Operating Temperature

Parameter	Symbol	Range	Unit	Notes
Operating Temperature	T_{CASE}	-40~85	°C	1

Note:

1. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the operation temperature range out of range mentioned in above table.

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11.3.3 ICC Characteristics

Parameter	Description	Test Conditions	Min	Typ*[1]	Max	Unit
I_{LI2}	Input Leakage Current Reset Signal High Only	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max	–	–	2	µA
I_{LI4}	Input Leakage Current Reset Signal Low Only *[2]	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max	–	–	15	µA
I_{CC1}	V_{CC} Active Read Current (-40°C to +85°C)	CS# = V_{IL}, @200 MHz, V_{CC} = V_{CC} max	–	12	20	mA
		CS# = V_{IL}, @250 MHz, V_{CC} = V_{CC} max	–	14	20	mA
I_{CC2}	V_{CC} Active Write Current (-40°C to +85°C)	CS# = V_{IL}, @200 MHz, V_{CC} = V_{CC} max	–	13	22	mA
		CS# = V_{IL}, @250 MHz, V_{CC} = V_{CC} max	–	15	22	mA
I_{CC5}	Reset Current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	–	–	550	µA
I_{CC6}	Active Clock Stop Current (-40°C to +85°C)	CS# = V_{IL}, RESET# = V_{IH}, V_{CC} = V_{CC} max	–	–	13	mA
I_{CC7}	V_{CC} Current during power up*[1]	CS# = V_{IH}, V_{CC} = V_{CC} max	–	–	35	mA
I_{DPD}	Deep Power Down Current (85°C)	CS# = V_{IH}, V_{CC} = V_{CC} max	–	–	12	µA

Parameter	Description	Test Conditions		Min	Typ*[1]	Max	Unit
I_{CC4}	V_{CC} Standby Current (-40°C to +85°C)	CS# = V_{IH}, V_{CC} = V_{CC} max	Full Array	–	80	1200	µA
			Bottom 1/2 Array	–	65	850	
			Bottom 1/4 Array	–	60	700	
			Bottom 1/8 Array	–	55	600	
			Top 1/2 Array	–	65	850	
			Top 1/4 Array	–	60	700	
			Top 1/8 Array	–	55	600	
I_{HS}	Hybrid Sleep Current (85°C)	CS# = V_{IH}, V_{CC} = V_{CC} max	Full Array	–	35	1100	µA
			Bottom 1/2 Array	–	30	800	
			Bottom 1/4 Array	–	25	600	
			Bottom 1/8 Array	–	22	500	
			Top 1/2 Array	–	30	800	
			Top 1/4 Array	–	25	600	
			Top 1/8 Array	–	22	500	

Notes:

1. Typical values are referring to the median average value measured @ T_{CASE}=25°C and for reference only, not tested in mass production process.
2. RESET# Low initiates exits from DPD state and initiates the draw of I_{CC5} reset current, making I_{LI} during Reset# Low insignificant.

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11.3.4 Power-Up Initialization

The HyperRAM device include an on-chip voltage sensor used to launch the power-up initialization process. V_{CC} and V_{CCQ} must be applied simultaneously. When the power supply reaches a stable level at or above V_{CC} (min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied on V_{CCQ} until V_{CC} (min) is reached during power-up, and then CS# must remain high for a further delay of t_{VCS}. A simple pull-up resistor from V_{CCQ} to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is Low during power up, the device delays start of the t_{VCS} period until RESET# is High. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

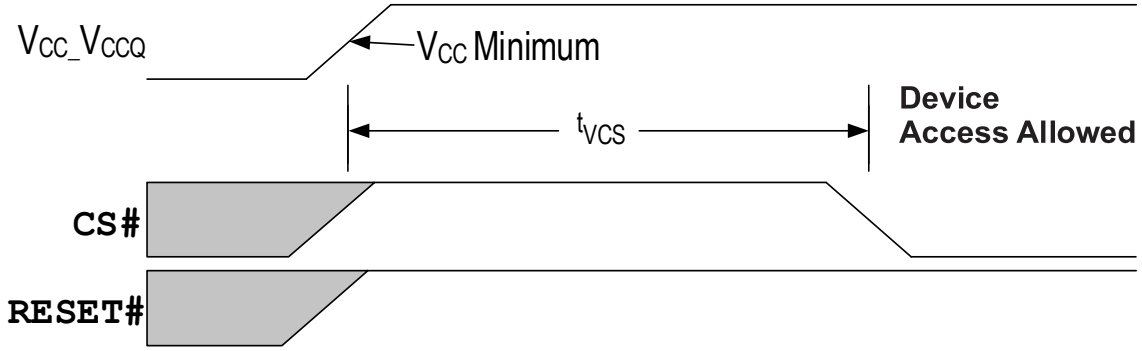


Figure 18 - Power-up with RESET# High

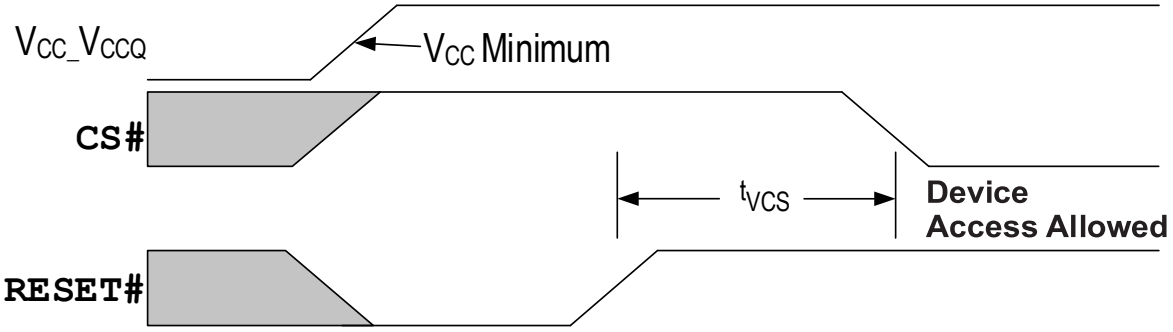


Figure 19 - Power-up with RESET# Low

Table 15 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
V_{CC}	V_{CC} Power Supply (typical 1.8V)	1.7	2.0	V
t_{VCS}	V_{CC} and V_{CCQ} ≥ minimum and RESET# High to first access	–	150	µS

Notes:

1. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).
2. V_{CCQ} must be the same voltage as V_{CC}.
3. V_{CC} ramp rate may be non-linear.

11.3.5 Power-Down

The HyperRAM devices are considered to be powered-off when the array power supply (V_{CC}) drops below the V_{CC} Lock-Out voltage (V_{LKO}). During a power supply transition down to the V_{SS} level, V_{CCQ} should remain less than or equal to V_{CC}. At the V_{LKO} level, the HyperRAM device will have lost configuration or array data.

V_{CC} must always be greater than or equal to V_{CCQ} ($V_{CC} \geq V_{CCQ}$).

During Power-Down or voltage drops below V_{LKO}, the array power supply voltages must also drop below V_{CC} Reset (V_{RST}) for a Power Down period (t_{PD}) for the part to initialize correctly when the power supply again rises to V_{CC} minimum. See Figure 20 - Power Down or Voltage Drop.

If during a voltage drop the V_{CC} stays above V_{LKO} the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If V_{CC} does not go below and remain below V_{RST} for greater than t_{PD}, then there is no assurance that the POR process will be performed. In this case, a hardware reset will be required ensure the HyperRAM device is properly initialized.

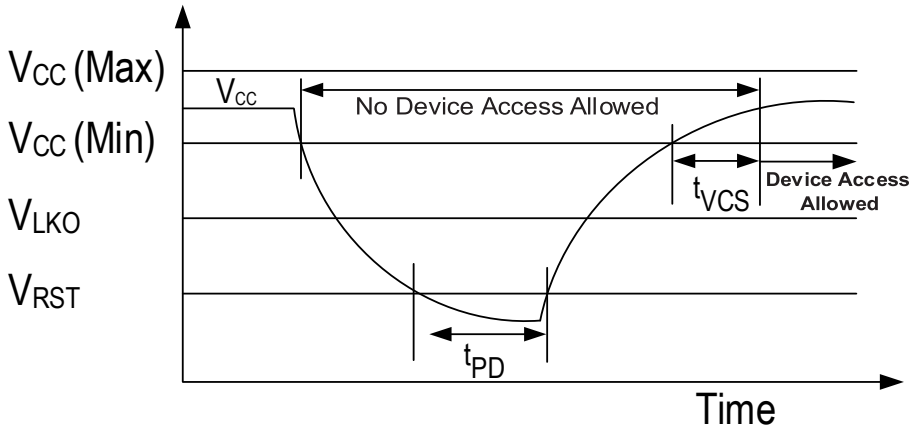


Figure 20 - Power Down or Voltage Drop

The following section describes HyperRAM device dependent aspects of power down specifications.

Table 16 - Power-Down Voltage and Timing

Parameter	Description	Min	Max	Unit
V_{CC}	V_{CC} Power Supply (typical 1.8V)	1.7	2.0	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	1.5	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.7	–	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	50	–	µS

Note: V_{CC} ramp rate can be non-linear.

11.3.6 Hardware Reset

The RESET# input provides a hardware method of returning the device to the standby state.

During t_{RPH} the device will draw I_{CC5} current. If RESET# continues to be held Low beyond t_{RPH}, the device draws CMOS standby current (I_{CC4}). While RESET# is Low (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A Hardware Reset will:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is low - memory array data is considered as invalid
- Force the device to exit the Hybrid Sleep state
- Force the device to exit the Deep Power Down state

After RESET# returns High, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# Low, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 12 - Array Refresh Interval per Temperature on page 25. This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume DRAM array data is lost after hardware reset and reload any required data.

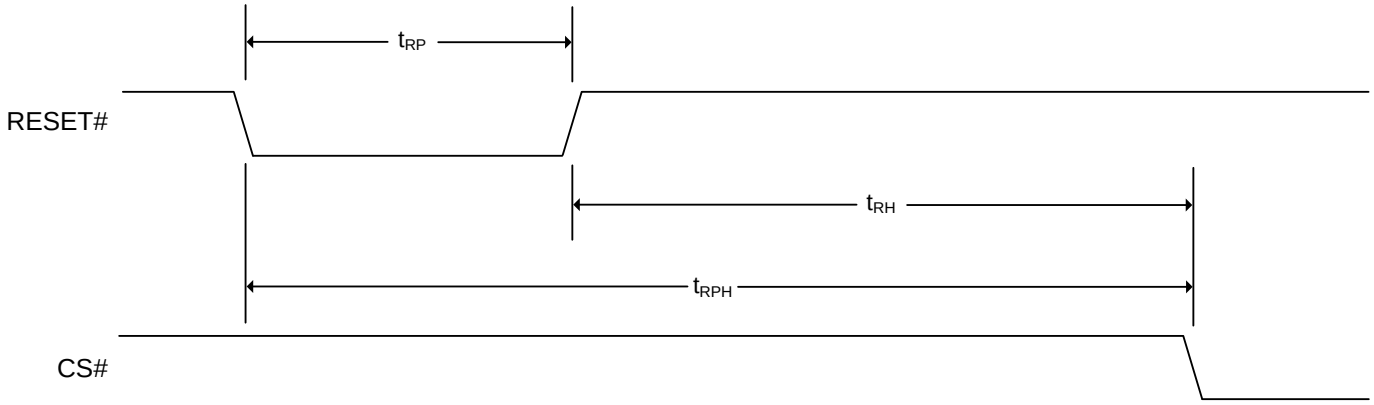


Figure 21 - Hardware Reset Timing Diagram

Table 17 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	–	nS
t_{RH}	Time between RESET# (High) and CS# (Low)	200	–	nS
t_{RPH}	RESET# Low to CS# Low	400	–	nS

11.3.7 Capacitance Characteristics

Table 18 - Capacitive Characteristics

Parameter	Description	Min	Max	Unit
C_I	Input Capacitance (CK, CK#, CS#)		3.0	pF
C_{ID}	Delta Input Capacitance (CK, CK#)		0.25	pF
C_O	Output Capacitance (RWDS[1:0])		3.0	pF
C_{IO}	IO Capacitance (DQx)		3.0	pF
C_{IOD}	IO Capacitance Delta (DQx)		0.25	pF

Notes:

1. These values are guaranteed by design and are tested on a sample basis only.
2. These values are applies to die device only (does not include package capacitance).
3. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, V_{CCQ} are applied and all other signals (except the signal under test) floating. DQ's should be in the high impedance state.
4. The capacitance values for the CK, CK#, RWDS[1:0] and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.

11.4 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may negative overshoot V_{SS} to -1.0V or positive overshoot to V_{CC} +1.0V, for periods up to 20 nS.

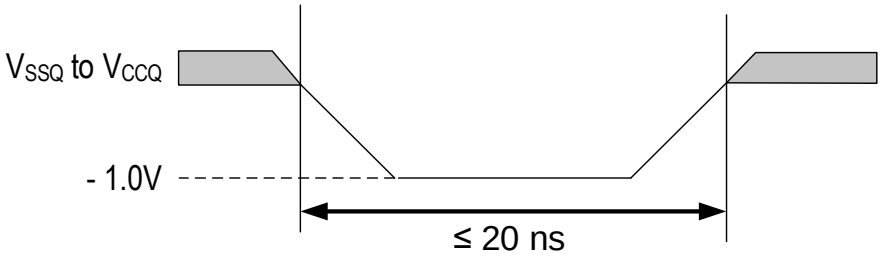


Figure 22 - Maximum Negative Overshoot Waveform

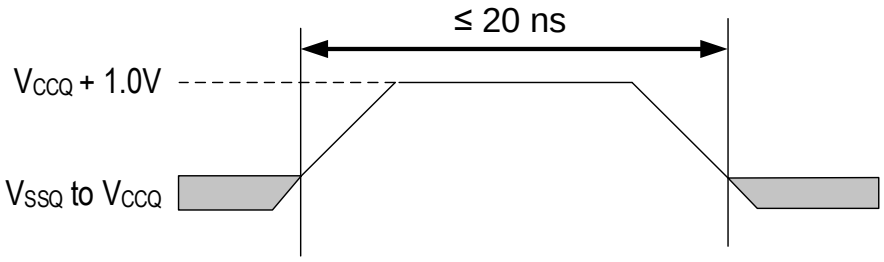
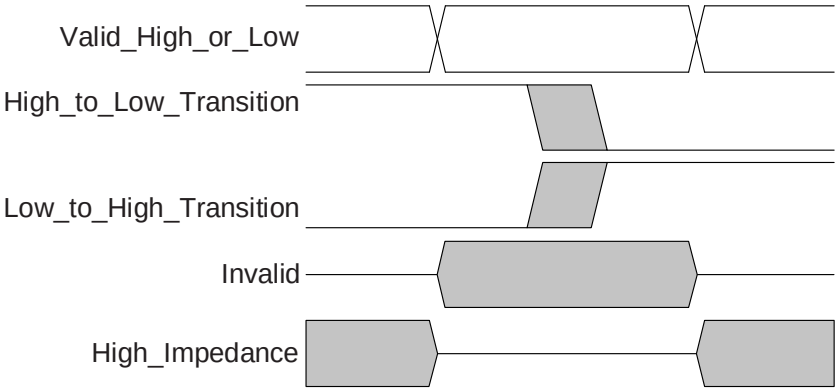


Figure 23 - Maximum Positive Overshoot Waveform

12. TIMING SPECIFICATIONS

The following section describes HyperRAM device dependent aspects of timing specifications.

12.1 Key to Switching Waveforms



12.2 AC Test Conditions

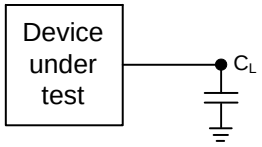


Figure 24 - Test load reference

Table 19 - Test Specification

Description	All	Unit	Notes
Output Load Capacitance, C_L	15	pF	
Minimum Input Rise and Fall Slew Rates	1.13	V/nS	1
Input Pulse Levels	0-V_{CCQ}	V	
Input timing measurement reference levels	V_{CCQ}/2	V	2
Output timing measurement reference levels	V_{CCQ}/2	V	2

Notes:

1. All AC timings assume this input slew rate.
2. Input and output timing is referenced to V_{CCQ}/2 or to the crossing of CK/CK#.

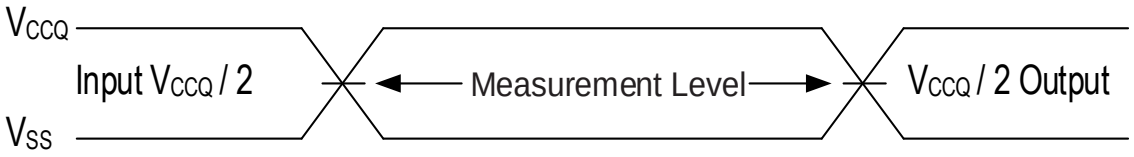


Figure 25 - Input Waveforms and Measurement Levels

Note: Input timings for the differential CK/CK# pair are measured from clock crossings.

12.3 AC Characteristics

12.3.1 Read Transactions

Table 20 - HyperRAM Specific Read Timing Parameters

Description	Parameter	250 MHz		200 MHz		166 MHz		133 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Chip Select High Between Transactions	tCSHI	6	–	6	–	6	–	7.5	–	nS
HyperRAM Read-Write Recovery Time	tRWR	35	–	35	–	36	–	37.5	–	nS
Chip Select Setup to next CK Rising Edge	tCSS	4	–	4	–	3	–	3	–	nS
Data Strobe Valid	tDSV	–	5	–	5	–	12	–	12	nS
Input Setup Time	tIS	0.5	–	0.5	–	0.6	–	0.8	–	nS
Input Hold Time	tIH	0.5	–	0.5	–	0.6	–	0.8	–	nS
HyperRAM Read Initial Access Time	tACC	28	–	35	–	36	–	37.5	–	nS
Clock to DQs Low Z	tDQLZ	0	–	0	–	0	–	0	–	nS
CK transition to DQ Valid	tCKD	1	5	1	5	1	5.5	1	5.5	nS
CK transition to DQ Invalid	tCKDI	0	4.2	0	4.2	0	4.6	0	4.5	nS
Data Valid (tDV min = tCKHP min - tCKD max + tCKDI max)	tDV	1	–	1.45	–	1.8	–	2.375	–	nS
CK transition to RWDS Valid	tCKDS	1	5	1	5	1	5.5	1	5.5	nS
RWDS transition to DQ Valid	tDSS	-0.4	+0.4	-0.4	+0.4	-0.45	+0.45	-0.6	+0.6	nS
RWDS transition to DQ Invalid	tDSH	-0.4	+0.4	-0.4	+0.4	-0.45	+0.45	-0.6	+0.6	nS
Chip Select Hold After CK Falling Edge	tCSH	0	–	0	–	0	–	0	–	nS
Chip Select Inactive to RWDS High-Z	tDSZ	–	5	–	5	–	6	–	6	nS
Chip Select Inactive to DQ High-Z	tOZ	–	5	–	5	–	6	–	6	nS
HyperRAM Chip Select Maximum Low Time (TCASE < 85°C)	tCSM	–	4	–	4	–	4	–	4	µS
Refresh Time	tRFH	28	–	35	–	36	–	37.5	–	nS
CK transition to RWDS Low @CA phase @Read	tCKDSR	1	5.5	1	5.5	1	5.5	1	5.5	nS

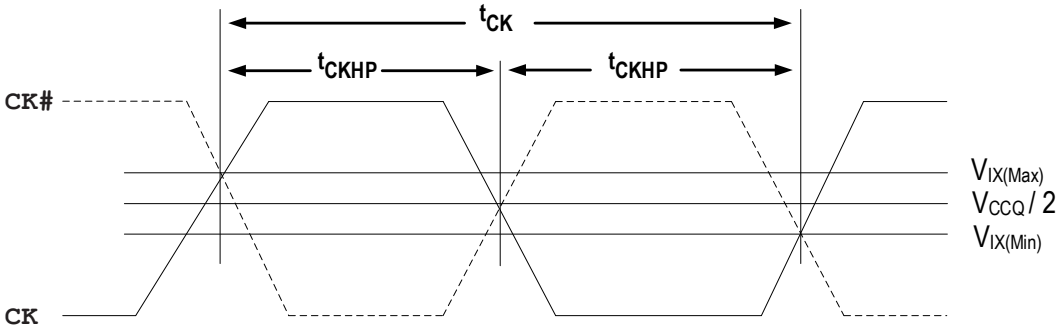


Figure 26 - Clock Characteristics

Table 21 - Clock Timings

Description	Parameter	250 MHz		200 MHz		166 MHz		133 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CK Period	tCK	4	100	5	100	6	100	7.5	100	nS
CK Half Period - Duty Cycle	tCKHP	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK Half Period at Frequency Min = 0.45 t_{CK} Min Max = 0.55 t_{CK} Min	tCKHP	1.8	2.2	2.25	2.75	2.7	3.3	3.375	4.125	nS

Notes:

1. Clock jitter of ±5% is permitted.
2. Minimum Frequency (Maximum t_{CK}) is dependent upon maximum CS# Low time (t_{CSM}), Initial Latency and Burst Length.
3. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the tCK and tCKHP out of range mentioned in above table.

Table 22 - Clock AC/DC Electrical Characteristics

Description	Parameter	Min	Max	Unit
DC Input Voltage	VIN	-0.3	VCCQ + 0.3	V
DC Input Differential Voltage	VID(DC)	VCCQ x 0.4	VCCQ + 0.6	V
AC Input Differential Voltage	VID(AC)	VCCQ x 0.6	VCCQ + 0.6	V
AC Differential Crossing Voltage	VIX	VCCQ x 0.4	VCCQ x 0.6	V

Notes:

1. CK and CK# input slew rate must be ≥1V/nS (2V/nS if measured differentially).
2. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
3. The value of VIX is expected to equal VCCQ/2 of the transmitting device and must track variations in the DC level of VCCQ.

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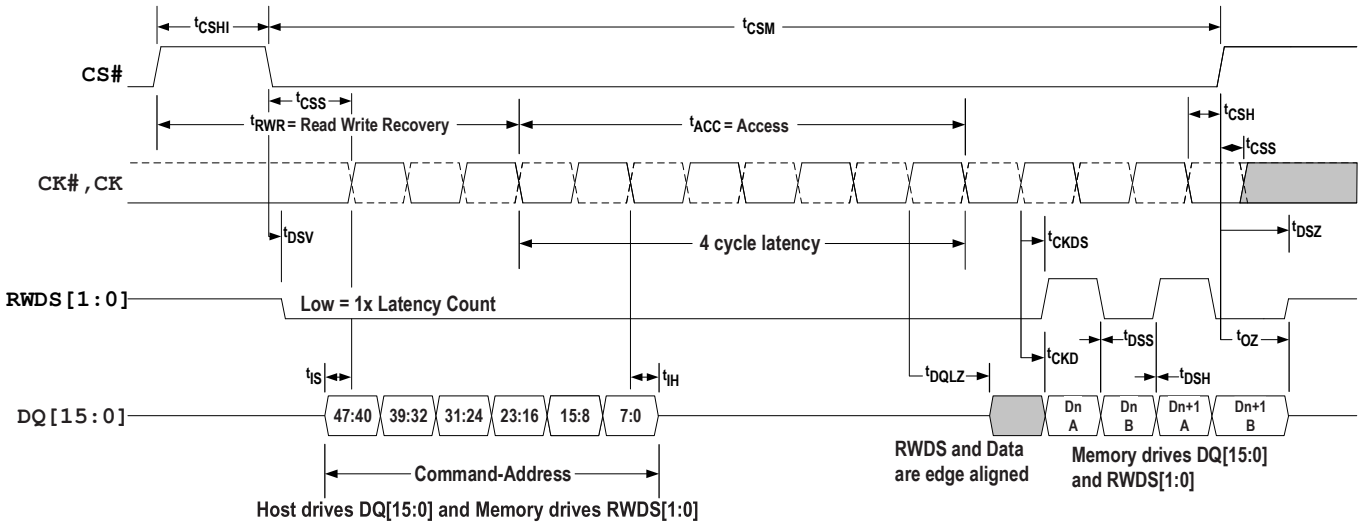

Figure 27 - Read Timing Diagram — No Additional Latency Required

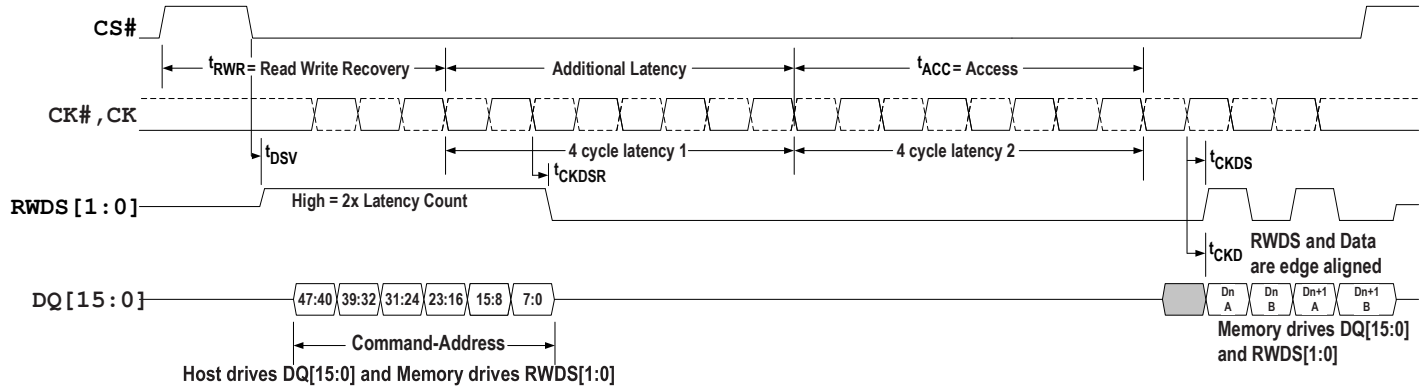

Figure 28 - Read Timing Diagram — With Additional Latency

Notes:

1. Timing parameters applicable to HyperBus-Extend-IO.
2. Transactions must be initiated with CK = Low and CK# = High.
3. CS# must return High before a new transaction is initiated.
4. The memory drives RWDS during the entire Read transaction.
5. Transactions without additional latency count have RWDS Low during CA cycles. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns low at t_{CKDSR}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycle latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
6. These parameters are required by HyperRAM.
7. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to “H” or “L”.

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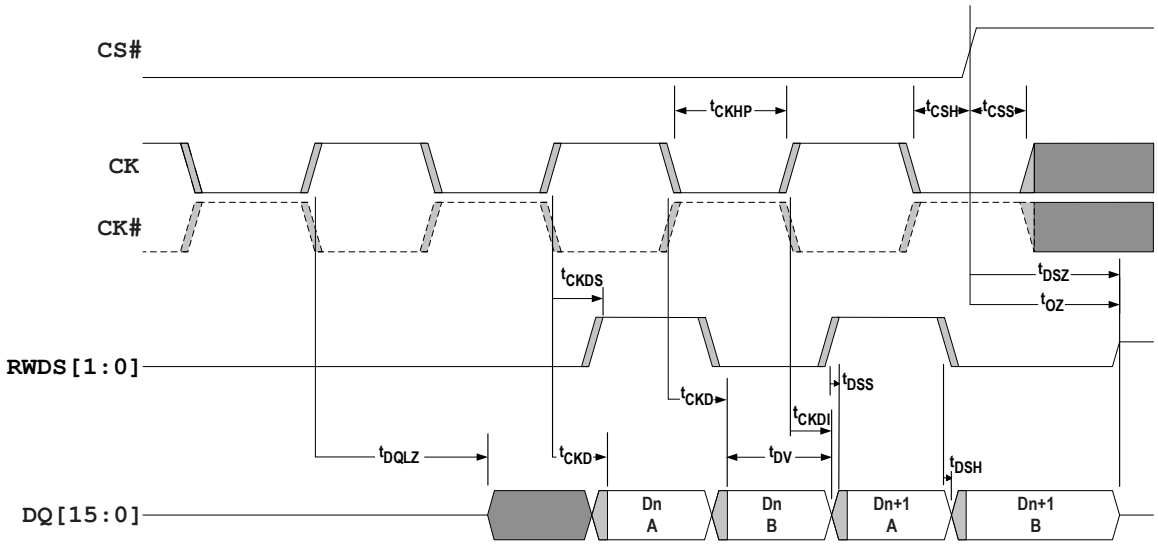

Figure 29 - Data Valid Timing

Notes:

1. This figure shows a closer view of the data transfer portion of read transaction diagrams to more clearly show the Data Valid period as affected by clock jitter and clock to output delay uncertainty.
2. The t_{CKD} and t_{CKDI} timing parameters define the beginning and end position of the data valid period.
3. The t_{DSS} and t_{DSH} timing parameters define how early or late RWDS may transition relative to the transition of data. This is the potential skew between the clock to data delay t_{CKD}, and clock to data strobe delay t_{CKDS}. Aside from this skew, the t_{CKD}, t_{CKDI}, and t_{CKDS} values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.

12.3.2 Write Transactions

Table 23 - Write Timing Parameters

Description	Parameter	250 MHz		200 MHz		166 MHz		133 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
HyperRAM Read-Write Recovery Time	t_{RWR}	35	–	35	–	36	–	37.5	–	nS
HyperRAM Read Initial Access Time	t_{ACC}	28	–	35	–	36	–	37.5	–	nS
Refresh Time	t_{RFH}	28	–	35	–	36	–	37.5	–	nS
HyperRAM Chip Select Maximum Low Time (T_{CASE} < 85°C)	t_{CSM}	–	4	–	4	–	4	–	4	µS
RWDS Data Mask Valid	t_{DMV}	0	–	0	–	0	–	0	–	nS

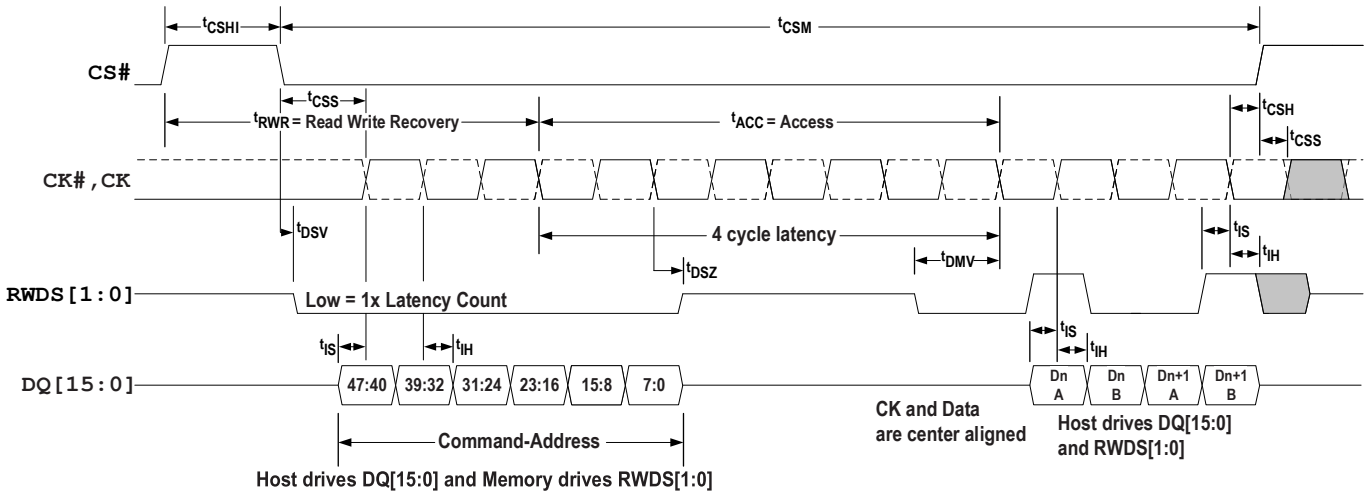

Figure 30 - Write Timing Diagram — No Additional Latency

Note: DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to “H” or “L”.

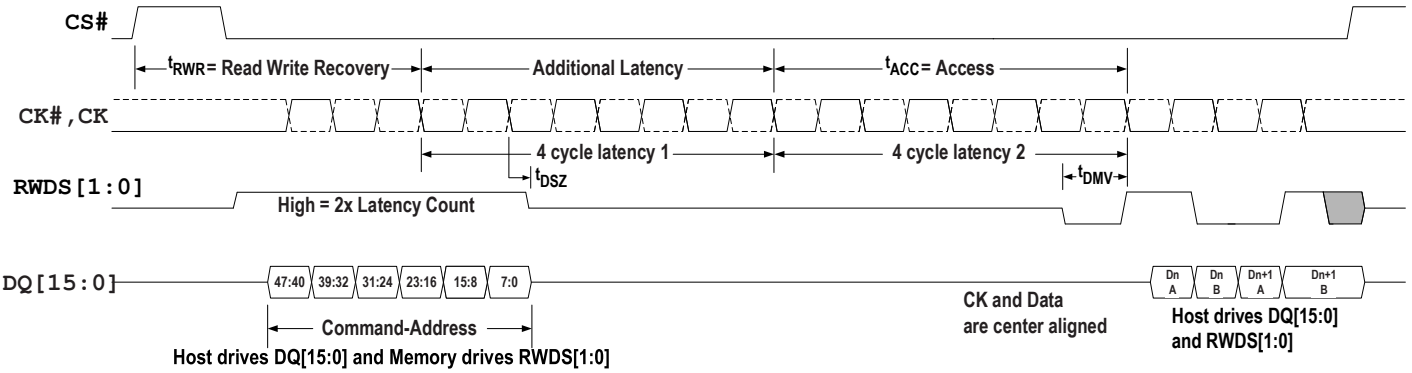

Figure 31 - Write Timing Diagram — With Additional Latency

Notes:

1. Timing parameters applicable to HyperBus-Extend-IO.
2. Transactions must be initiated with CK=Low and CK#=High. CS# must return High before a new transaction is initiated.
3. During write transactions with latency, RWDS is used as an additional latency indicator initially and is then used as a data mask during data transfer.
4. Transactions without additional latency count have RWDS Low during CA cycles and RWDS returns Hi-Z at t_{DSZ}. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns Hi-Z at t_{DSZ}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycle latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
5. At the end of Command-Address cycles the memory stops driving RWDS to allow the host HyperBus-Extend-IO master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave. This can be done during the last cycle of the initial latency.
6. The write transaction shown demonstrates the Dn A(16-bits) and the Dn+1 B(16-bits) being masked. Only Dn B(16-bits) and Dn+1 A(16-bits) are modified in the array. Dn A(16-bits) and Dn+1 B(16-bits) remain unchanged.
7. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to “H” or “L”.

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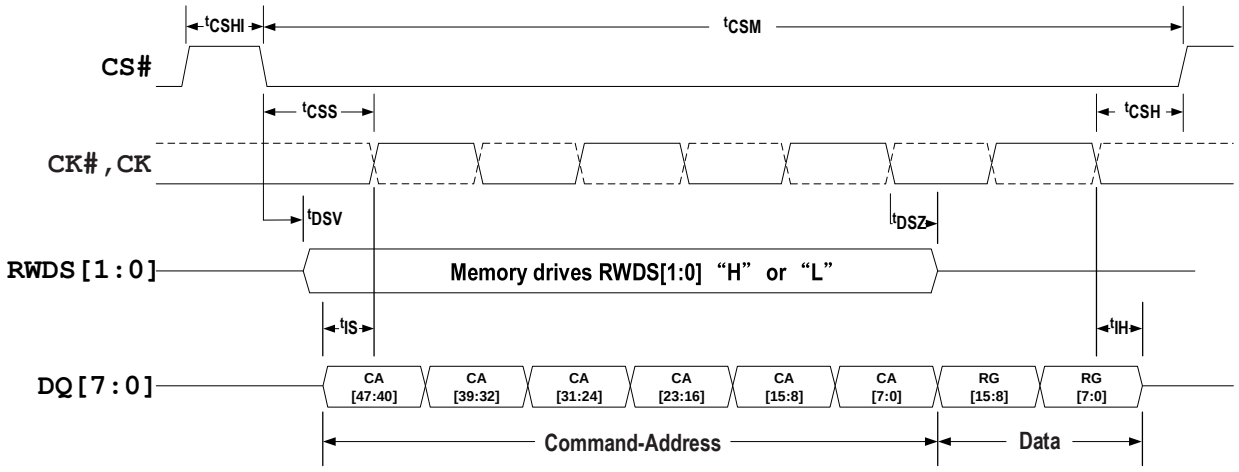


Figure 32 - Write Operation without Initial Latency (Register Write)

Notes:

1. Transactions must be initiated with CK=Low and CK#=High. CS# must return High before a new transaction is initiated.
2. Writes without Initial Latency, do not have a turnaround period for RWDS. The slave device will always drive RWDS during the Command-Address period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the slave device has received the first byte of CA, that is, before the slave knows whether the transaction is a read or write, to memory space or register space. In the case of a write without Initial Latency, the RWDS state during the CA period does not affect the Latency of Register Write. Since master write data immediately follows the Command-Address period in this case, the slave may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Register Write. Register Write do not use RWDS as a data mask function. All bytes of write data are written (full word writes).
3. DQ[15:8] input will be not used for command/Address decoding or as the write data, however, the controller has to drive DQ[15:8] to "H" or "L".

12.3.3 Hybrid Sleep Timings

Table 24 - Hybrid Sleep Timing Parameters

Description	Parameter	Min	Max	Unit
Hybrid Sleep CR1[5]=1 register write to Hybrid Sleep power level	tHSIN	–	3	µS
CS# Pulse Width to Exit Hybrid Sleep	tCSHS	60	3000	nS
CS# Exit Hybrid Sleep to Standby wakeup time	tEXTHS	–	100	µS

Note:

1. After exit Hybrid Sleep command effective. the host must wait for at least 100µS to do the next valid command to the HyperRAM device.

12.3.4 Deep Power down Timings

Table 25 - Deep Power down Timing Parameters

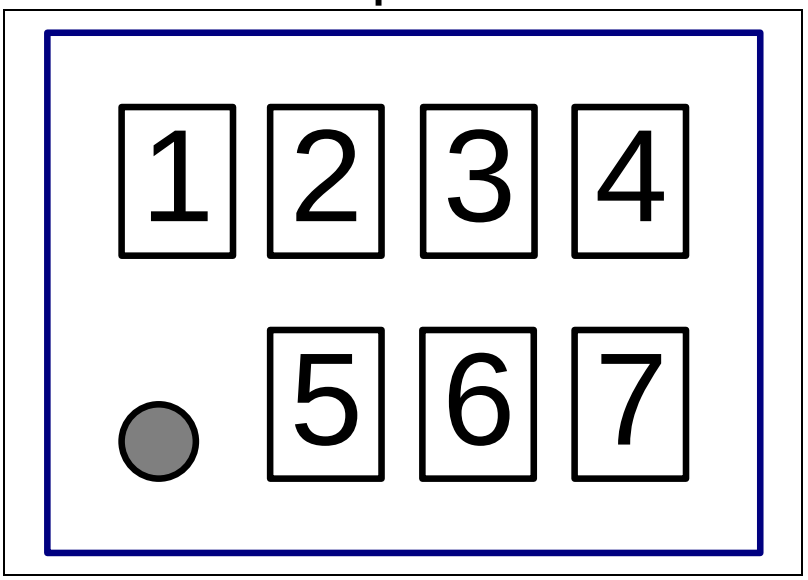
Description	Parameter	Min	Max	Unit
Deep Power Down CR0[15]=0 register write to DPD power level	tDPDIN	–	3	µS
CS# Pulse Width to Exit DPD	tCSDPD	200	3000	nS
CS# Exit Deep Power Down to Standby wakeup time	tEXTDPD	–	150	µS

Note:

1. After exit DPD command effective. the host must wait for at least 150µS to do the next valid command to the HyperRAM device.

13. W958D6NW WLCSP 30 BALL PACKAGE MARKING COMPOSITION

Top View



- **Digit 1: Part number code**

Part number code for part number

Code	Part number
1	-
2	W958D6NWSX5I
3	-
4	-
5	-
6	-
7	W958D6NWSX4I

- **Digit 2, 3, 4: Serial number**

- **Digit 5: Year code**

Year code for year (For year 2020 to 2029)

Code	0	1	2	3	4	5	6	7	8	9
Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029

- **Digit 6, 7: Week code**

Week code for week (Week by calendar year)

Code 6, 7	01	02	03	……	31	32	……	53	54
Week	1st week	2nd week	3rd week	……	31th week	32th week	……	53th week	54th week

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14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01-001	Jun. 04, 2021	All	Initial formal datasheet
A01-002	Sep. 30, 2021	5	Refine RWDS[1:0] Read Write Data Strobe description of section 4
		36, 37, 39	Add 166 and133MHz AC parameters timing spec
		36	Revise data valid calculation formula as below (t_{DV} min = t_{CKHP} min - t_{CKD} max + t_{CKDI} max)
		30	Revise note #1 typical I_{CCX} values definition
		30	Add I_{CC1} & I_{CC2} typical spec values
		30	Add 1/2, 1/4 & 1/8 Array of I_{CC4} & I_{HS} typical spec values
		30	Revise Full Array of I_{CC4} & I_{HS} typical spec values
A01-003	Nov. 16, 2021	43	Add WLCSP 30 ball package marking composition information
A01-004	Jan. 14, 2022	1	Revise title to 256Mb HyperRAM 3.0 x16 pSRAM
		3	Revise Interface in feature list (HyperBus-Extend-IO ==> HyperBus-Extend-IO (HyperRAM 3.0)
		3	Revise Interface in order information (HyperBus-Extend-IO ==> HyperBus-Extend-IO (HyperRAM 3.0))
		7	Add explanation for the term of HyperRAM 3.0
		11	Remove note #3 of Table 2 - Command/Address Bit Assignments
		18	Refine “Row” and “Half-Page” notes description of Table 3 - Memory Space Address Map
		18	Remove redundant “For example:” wording in last paragraph of section 8.2
		20	Revise Device Type of ID1[3:0] (HyperRAM-Extend-IO ==> HyperRAM 3.0)
		26	Revise Table 13 - Interface States V_{CC} / V_{CCQ} min ==> ≥ V_{CC} / V_{CCQ} min
		27	Refine last paragraph description of section 10.2.1
		41	Add note #3 for Figure 32
		41	Add note for Table 24 - Hybrid Sleep Timing Parameters
		41	Add note for Table 25 - Deep Power down Timing Parameters
A01-005	Jun. 27, 2022	30	Revise I_{CC6} spec value (25mA ---> 13mA)
		41	Refine note #2 for Figure 32
A01-006	Nov. 25, 2022	3, 21, 23, 30, 36, 37, 39, 43	Add 250MHz part number in order information table with related 250MHz description and DC/AC spec in this datasheet
A01-007	Mar. 14, 2023	42	Remove package outline drawing figure and dimensions spec portion and move it to another separated W958D6NW 256Mb HyperRAM 3.0 x16 WLCSP 30 package information document

Note: The content of this document is subject to change without notice.

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